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**Invited**

# A System Chip Innovation by the Ferroelectric Memory Technology

**Isao Matsumoto**
Device Technology Div. ULSI Research and Development Headquarters, ROHM CO.,LTD.
21, Saiin Mizosaki-cho,Ukyo-ku, Kyoto 615-8585, Japan
TEL : 81-75-311-2121 FAX : 81-75-311-8963 e-mail : matsumoto@rohm.co.jp

## 1. Introduction

The needs for lower power and non-volatility on memory devices are increasing by the magnifying demand for portable electronic apparatuses such as mobile phones.

PDA requires not only higher speed access but also higher speed writing. The conventional non-volatile memories have limited endurance up to 1 million cycles, which is not enough for the variety of applications using non-volatile memories.

The ferroelectric memory has clear advantages such as non-volatility, lower power conumption, higher endurance on writing cycles and higher writing speed.

## 2. Features of Capacitor type of Ferroelectric Memories

Conventional non-volatile memories are ROM type only, and are used for limited application area. On the other hand, ferroelectric memories are non-volatile RAM, and will provide wider application field than existing conventional memories.

The ferroelectric memory has the feature as a non-volatile RAM. Writing endurance cycle has been reached up to $10^{10}$-$10^{13}$ cycles. The recent works of $SrBi_2Ta_2O_9$ [1] ferroelectric material or $IrO_2$ electrode [2] have improved the fatigue of switching charge amount, and indicate even more than $10^{12}$-$10^{13}$ cycles can be achievable. 100nsec writing speed of FRAM is almost same level as SRAM and DRAM, it is much faster than the writing speed of conventional non-volatile memory.

The ferroelectric memory is operated at 3V now, it will be operated at 1.5V in the near future. Because 1.5V saturation on P-E hysteresis curve has been reported.

At the present time, the cell size of ferroelectric memory is not small enough, because the ferroelectric process technology is not well established yet for a half micron level patterning.

But, once fine process technology becomes available, ferroelectric memories will have potential to achieve a cell size compatible to a DRAM cell size with 1T1C cell in comparison with the same design rule. When 1T (1 transistor) cell become available, the size will be close to a cell size of a flash memory.

## 3. MFMIS FET

Ferroelectric memory FETs with a metal-ferroelectric-semiconductor (MFS) structure have already been reported [3,4]. However it is difficult to deposit ferroelectric thin films directly on a Si substrate. Pb, Ti and other elements diffuse into the Si substrate, and unnecessary SiO2 layers are formed during thermal treatment. To solve these problems, a buffer layer between the Si and the ferroelectric layer has been considered. A metal - ferroelectric - insulator - semiconductor (MFIS) structure has also been studied, which has an insulator as a buffer layer.

However, in this structure, the voltage of the ferroelectric is only a slight part of the applied voltage, especially when the dielectric constant of the ferroelectric is high. Therefore the MFMIS FET requires a low dielectric constant to apply sufficient electric field for polarization reversal of the ferroelectric thin film layer.

SNO family have low dielectric constant (43～75). And it is hard to degrade in hydrogen ambience, because of high melting point.

MFMIS cells using STN capacitors ($Pt/STN/Pt/IrO_2$) are succeeded to be operated with low voltage. When the applied voltage was $\pm$5V, memory window of 3.8V was obtained. In addition the silicide formation of Pt during the crystallization annealing was blocked by the $IrO_2$ layers.

## 4. FRAM Embedded Application

The features of ferroelectric memories are not only replacing the existing memory market, but also creating new application fields, and are impacting the society.

As the importance of ecology is increasing, ferroelectric memories will be getting more important position between the memories. For example, battery back SRAM will be replaced by ferroelectric memories, because of the disposition of used batteries. A ferroelectric memory has more advantages as a memory embedded product than other conventional memories, because of its non-volatile, high speed writing / programming, low power supply voltage, high endurance and good CMOS process adaptability. Ferroelectric memory embedded RF-ID tag / contactless smart IC cards are one of the most adequate examples.

Recently, flash memory embedded system LSI chips are getting popular, especially flash memory embedded CPUs are used to many electronic systems. A simulteneous multi-process implementation for a fine electronic control is required in a recent system. As a performance of software algorithm gives more influence to a system, a development work of algorithm takes more time. Under these circumstances, conventional mask ROM embedded type CPUs have more difficult situation for a short development cycle, because of a revised LSI have to be made again to change ROM when a software has a bug.

If mask ROM is replaced to flash memory, a LSI is able to be manufactured without waiting a completion of software development. An algorithm installation to a CPU shall be done just before fab out a final product set by writing the program to the flash memory embedded to a LSI chip.

In additional, flash embedded architecture enables to upgrade a software without changing the LSI chip.

In further, if FRAM is applied as embedded ROM and RAM for CPU, in system programming becomes reality, because of using the features of FRAM such as high speed/low power programming.

It is not far away to change a software or to have learning function and takes the learning results in the system to change a configuration of a system.

## 5. A New Device Architecture

Recently, it is demonstrated that utilizing STN($Sr_2$ (Ta, $Nb)_2O_7$), possessing relatively low dielectric constant and superior immunity to process degradation [5], for ferroelectric layer in the MFMIS FET makes integration of such MFMIS FET into conventional wafer process sufficiently practical.

The ferroelectric memory that consists of such ferroelectric FET can be embedded in Logic LSIs and function as the nonvolatile switching devices as well as realize standard Memory LSIs.

Today, the integration level of ULSI is getting extremely high, up to several million transistors on a chip, and by 2010 one billion transistors will be integrated.

Such a super high integrated chip will never be produced economically without having any redundancy circuit on it.

But this problem will be solved by the FPGA approach, because a redundancy function is easily introduced to the MFMIS FET. The ferroelectric memory technology enables the use of a smaller switch memory cell to be compared to conventional SRAM based FPGA, and no back-up memory is required with ferro memory based FPGA.

The small cell of FPGA with the ferroelectric memory will spread to more than 500K gate count of FPGA with fine cell architecture similar to gate array.

This ferroelectric memory based FPGA can have a good security function to protect from having the circuit copied. Further, a more important feature of this FPGA is that it will take self learning results into the logic circuit configuration during operation in a system, because of its high speed programming and no additional high voltage power supplied requirement on the board. This ferroelectric memory FPGA can be used as DPGA (dynamic programmable gate array), and in system programming of a hardware VIA telecommunication line will become available by using DPGA technology.

The ferroelectric memory technology will lead to a new semiconductor device architecture, including a neuron device using ferroelectric memories as analog memory, and will take the major place in the coming multi- media era.

## 6. Conclusion

The ferroelectric memory technology will give a big impact to the existing semiconductor memories, and open new application fields, which will change our life style. Also, the technology will enable new device architectures for the 21st century.

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