Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 50-51

Conformal Step Coverage of (Ba,Sr)TiO$_3$ Films Prepared by Liquid Source CVD Using Ti(t-BuO)$_2$(DPM)$_2$

Takaaki Kawahara, Shigeru Matsuno, Mikio Yamamuka, Masayoshi Tarutani, Takehiko Sato, Tsuyoshi Horikawa, Fusaoki Uchikawa and Kouichi Ono

Advanced Technology R&D Center, Mitsubishi Electric Corporation,
8-1-1 Tsukaguchi-Honmachi, Amagasaki, Hyogo 661-8661, Japan
Phone: +81-6-497-7099, Fax: +81-6-497-7288, E-mail: kawahara@apr.crl.melco.co.jp

1. Introduction

(Ba,Sr)TiO$_3$ [BST] films with high dielectric constant have been studied as a capacitor dielectric in Gbit-scale DRAMs [1-3]. We demonstrated a simple stacked capacitor structure with Ru/BST/Ru for 1Gbit DRAMs [1]. In the fabrication of the capacitor, a two-step deposition process with low substrate temperatures was applied for BST film formation by liquid source CVD, and the deposition process was confirmed to result in smooth surface and high step coverage of 75% at an aspect ratio of 1.4 [4, 5].

In 4Gbit DRAMs, a storage node higher than 0.36 μm will be demanded to achieve a capacitance $\geqq$25 fF/cell for a projection area of 0.051 μm^2 and a spacing of 0.13 μm, along with an equivalent SiO_2 thickness (t_{eq}) of 0.50 nm. This, in turn, requires the conformal step coverage more than 80% at an aspect ratio of $\geqq$3 for capacitor dielectrics with $t_{eq} \leqq 0.50$ nm (Fig.1).

Recently, Ogi *et al.* have investigated the reaction of a new Ti CVD source, Ti(*t*-BuO)$_2$(DPM)$_2$ [bis (*t*-butoxy) bis (dipivaloylmethanato) titanium] [6]. They found that the source was more stable in THF [tetrahydrofuran, C_4H_8O] solution and also in vapor phase than conventional sources such as TiO(DPM)$_2$, and pointed out that the sticking probability of the precursor might be smaller than the others. Thus, the Ti source Ti(*t*-BuO)$_2$(DPM)$_2$ is expected to give the improved step coverage of BST films.

In this paper, we present the step coverage of BST films using Ti(*t*-BuO)$_2$(DPM)$_2$, and their electrical properties with and without post-annealing [7].

2. Experimental

The BST-CVD system consisted of a single-wafer, low-pressure thermal CVD reactor, a vaporizer for liquid source materials, and a shower-type gas nozzle [4]. In this study, Ba(DPM)$_2$, Sr(DPM)$_2$ and Ti(*t*-BuO)$_2$(DPM)$_2$ dissolved in THF were used for liquid source materials. Figure 2 shows the molecular structure of Ti(*t*-BuO)$_2$ (DPM)$_2$, developed by Mitsubishi Materials Corp. [6], which is more stable in THF solution and also in vapor phase because Ti ion is surrounded by four large organic ligands. BST films were deposited by two-step deposition technique [5], at a substrate temperature T_s = 430 ℃ and a reactor pressure P = 5 Torr.

3. Results and Discussion

Figure 3 shows the step coverage of BST films using Ti(*t*-BuO)$_2$(DPM)$_2$, having no overhang on the upper corner and a high step coverage of d_{min}/d_{max} = 70% for an aspect ratio of D/W = 5. Moreover, an excellent coverage of 80% was obtained at an aspect ratio of 3.3, which was much better than that of 50% using TiO(DPM)$_2$. These data are plotted in Fig.4, where the results of Monte Carlo simulation are also shown for several sticking probabilities β [5]. A comparison between the experimental and numerical results indicates that β are 0.02 and 0.1 in cases using Ti(*t*-BuO)$_2$(DPM)$_2$ and TiO(DPM)$_2$, respectively, and that the step coverage is significantly improved by using Ti(*t*-BuO)$_2$(DPM)$_2$.

Figure 5 shows *I-V* curves of BST films with and without post-annealing in N_2 (750 ℃, 30 min) after two-step deposition, where the film (Ba+Sr)/Ti ratio and thickness are 0.8 and 30 nm, respectively. The voltage giving a leakage current $J_L = \pm 2x10^{-7}$ A/cm^2 deteriorates from +2.8 to +2.0 V and from −3.0 to −2.3 V through post-annealing; however, the t_{eq} value decreases from 0.94 to 0.58 nm. Figure 6 shows the relationship between the t_{eq} and film thickness with and without post-annealing, where the (Ba+Sr)/Ti ratios and thicknesses are 0.9 - 1 and 24 - 38 nm, respectively. After post-annealing, the t_{eq} values are less than 0.5 nm, for BST films less than 30 nm in thickness, and t_{eq} = 0.44 nm is achieved for 24-nm-thick films.

4. Conclusions

The step coverage and electrical properties of BST films prepared by liquid source CVD have been studied using Ti(*t*-BuO)$_2$(DPM)$_2$. The new Ti source Ti(*t*-BuO)$_2$ (DPM)$_2$ gave the improved step coverage of 80% and 70% for the aspect ratio of 3.3 and 5, respectively, and t_{eq} = 0.44nm was obtained for the film thickness of 24nm after post-annealing. These characteristics meet the requirements of the capacitor for 4Gbit DRAMs.

References

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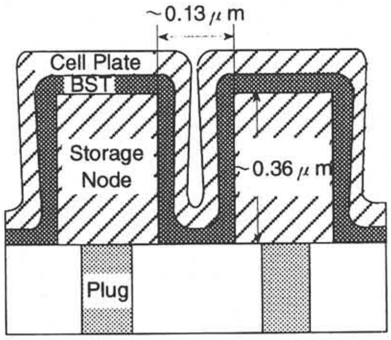

Fig.1 Schematic sectional view of Ru/BST/Ru capacitors used for 4Gbit DRAMs.

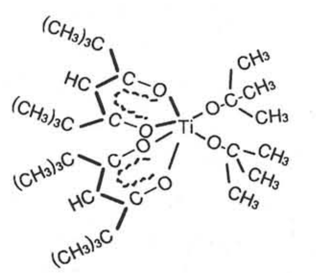

Fig.2 Molecular structure of a new Ti CVD source $Ti(t\text{-}BuO)_2(DPM)_2$ for BST film deposition.

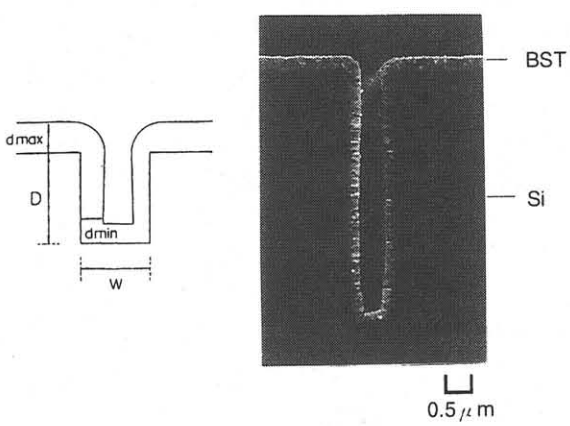

Fig.3 Step coverage of 70% of CVD-BST films using $Ti(t\text{-}BuO)_2(DPM)_2$ for an aspect ratio of 5.

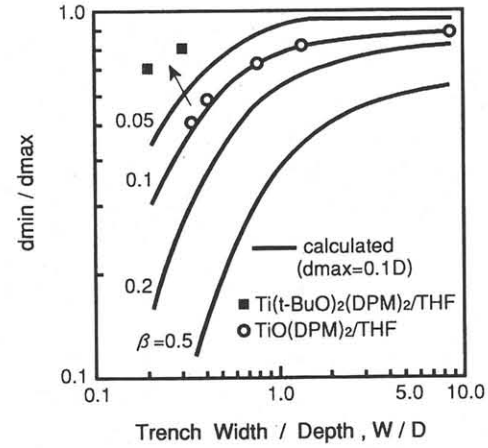

Fig.4 Plots of the measured d_{min}/d_{max} versus W/D for BST films using $Ti(t\text{-}BuO)_2(DPM)_2$ and $TiO(DPM)_2$. Here, solid lines represent the results of Monte Carlo simulation at $d_{max} = 0.1D$ for several sticking probabilities β.

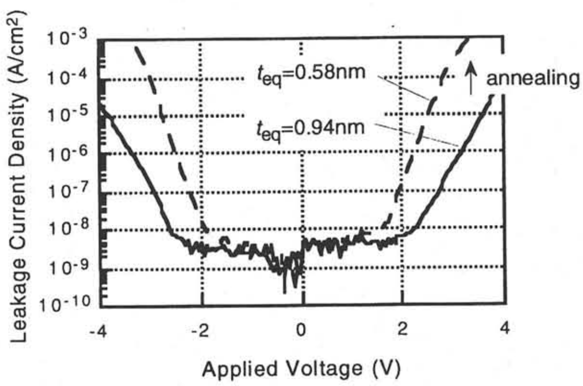

Fig.5 *I-V* curves of BST films with and without post-annealing. The film composition ratio and thickness are (Ba+Sr)/Ti = 0.8 and 30 nm, respectively.

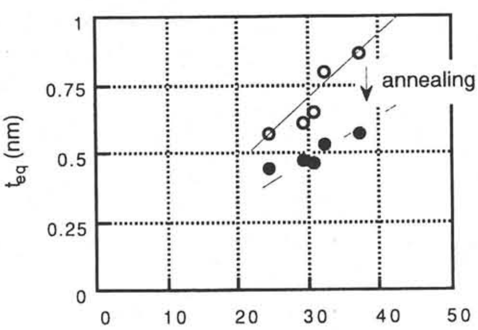

Fig.6 Relationship between t_{eq} and thicknesses of BST films with and without post-annealing. The film composition ratios of BST films is in the range (Ba+Sr)/Ti = 0.9 - 1.0.