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Invited

Guide-Lines on Flash Memory Cell Selection

Kuniyoshi Yoshikawa

Micro & Custom LSI Division, Microprocessor Product engineering Dept. Toshiba Corporation
1, Komukai-Toshiba, Saiwai-ku, Kawasaki 210, Japan e-mail :yosikawa@tmamoa.tama.toshiba.co.jp

1. Introduction

Recently the needs for flash embedded logic devices is rapidly increasing, while flash technology development. has been done by focusing on standalone high density memories. Since key concerns and required specification are not the same, chosen cell technology can be different from each other. Even for standalone memories, more than 10 variations are existing, and no sign is seen for its technology convergence. Furthermore, increasing scaling mismatch between flash and logic devices makes it more difficult to realize cost effective solution. Therefore, clear guide-lines on flash technology selection is strongly desired for coming 0.25μm and the beyond. In this talk, important key issues for flash devices will be addressed with discussing various pros and cons associated with technology selection, focusing on flash embedded application.

2. Key Concerns

Program/Erase (P/E) method

Only available methods for electron injection are tunneling and hot electron injection. The former needs high electric field(<10MV/cm) and the later requires sufficient electron energy to surmount SiO_2/Si barrier. The choice is closely related to oxide reliability, cell structure, array architecture as well as product specifications. Important criteria is bit-by-bit charging speed, power consumption and random charging capability. Table 1 shows various bit-by-bit alterable P/E methods. Uniform-FN tunneling is the best for power budget, but is not suitable for random operation. Edge-FN tunneling to/from junction & band-to-band tunneling(BTBT) can realize low power and bit-by-bit random operation. BTBT induced hot hole damage on oxide can be prevented by P-channel cell. Conventional channel hot electron(CHE) injection realizes the fastest charging speed, but will not be appropriate for very low power portable application.

Cell and Array structures

Density requirement greatly affects the choice of 1Tr/cell and 2Tr/cell(or split-gate). For stand-alone high density memories, 1Tr/cell like ETOX or NAND will be inevitable. On the contrary, for flash embedded logic devices, NOR-based array architecture is essential and simple P/E method and control CKTs are more important . In addition, process and library compatibility with logic CMOS is the key.

High speed random accessibility will become more and more concerns to match with peripheral CPU speed. Pass transistor in the array will be indispensable to minimize bitline-delay, while WL-delay can be reduced by Metal strap or salicide. Vt of cell's "1" state should be close or below zero to realize near direct Vcc of WL. Therefore, 2Tr/cell or split-gate approaches will comeback in low voltage, low power applications with medium density.

Reliability

Reliability assurance is the must for all NV devices. Currently, charge retention capability and read-disturb immunity after P/E cycling are the most important concerns in flash devices[1]. Since intrinsically reliable cell should be chosen for every application, hot holes created by P/E operation should be minimized. Since n-ch edge-FN tunneling concept for bit-by-bit operation has inherent hole damage difficulty, uniform-FN or P-ch BTBT electron injection or Poly-poly tunneling cells are the candidates. For simplicity, p-ch BTBT electron injection is the best.

Over-erase and erratic bit problems are also minimized. Bit-by-bit control capability should be prepared for 1Tr/cell structure. Again, 2Tr/cell will provides easier solution with less CKT complexity, which can reduce control CKT area.

Fabrication Process

Process simplicity and compatibility with logic CMOS become more important to embedded devices. Simple S/D structure and less additional mask #s are strongly desired. From this, uniform-FN tunneling for block operation is preferable. For fast bit-by-bit charging, BTBT is very effective, because no sophisticated S/D engineering is required. Moreover, it is strongly desirable to realize EE+Flash cells with the same process. Both cells are requested to operate with the same Vpp. If both use the same P/E method, this is the best. The candidates are again edge-FN or BTBT.

3. Future direction

Current flash cell structure and its operation have fundamental limitation as shown in Table 2. Technology breakthrough is strongly required for future flash survival.

Table 2. Flash limitations and possible solution[6]

	Issues	Solution??
P/E mechanism/speed FN --- High Field(>10MV/cm) for Tunnel CHE --- High Voltage(>~5V) to create Hot Electron	< 5~10V for fast write Ox. thickness irrelevant	Mechanism change! *Polarization (Ferro?)* *Direct Tunnel (SET?)*
Storage Structure Floating Gate --- Continuous	Ox. defect/yield/ reliability	ECC for High density *Discrete Traps (MNOS?)* *Multiple dots (SET?)*
Storage Insulation Tunnel ox > Direct tun. limit (Insulation & electron path)	SILC after Cycling Max. Cycle~1M	No way below 8nm ox. New dielectric *Coulomb Blockade with <5nm (SET?)*
Scaling/Higher density Active area scaling hard! Multilevel >2~3 bits/cell	Fluctuation Control	ECC for specific market

Multi bits/Cell

Basically there are two ways to realize multi bits/cell. The one is multi-level(ML) [2]Vt storage in the same cell and the other is multi-storage(MS)[3] which uses different physical locations to store charge in one cell. The former needs precise Vt control, sensing and better reliability, and generally performances are not fully compatible with single bit/cell devices. Actual products using 2bits/cell are available and effectively, 4~5F^2/bit is realized. But, in general, ML is too complicated for embedded devices

The latter concepts will be more important since it only requires improved sensing, while Vt control and reliability specification are the same as conventional one. In addition, MS can be combined with ML which further improves the density to 2~2.5F^2/bits.

Alternative dielectric

In order to overcome a current scaling limitation of SiO_2 and realize effective scaling, non-SiO_2 based new tunnel dielectric should be introduced. That should have higher dielectric constant to achieve 2.5-3nm equivalent oxide thickness with preventing direct tunneling as well as reasonable barrier height to suppress thermal exited charge conduction. The film also has less trapping characteristics and immunity against carrier injection. One candidate is high quality silicon nitride like JVD-nitride which shows less trapping and less SILC[4], .

Storage structure

Poly-Si floating gate has been used as a storage node so far, but this continuous FG structure is not robust enough against single oxide defect and SILC. Charge storage in discrete traps(sites) like SONOS will play more important role in future technology, because it allows oxide defects and hot-hole induced SILC without affecting majority of stored charge.

4. Summary

Key issues for flash cell selection were discussed based on technological point of view. Future important technology items were also addressed.

In real, company's technological history and resource minimization policy greatly affect the choice of the cell. But it should be noted that no ultimate unified cell technology for all applications is available now. Therefore, clever cell selection should be done for each market requirements to gain strong cost effective solution.

References

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Table 1. Bit alterable operation comparison

Tr. type	Mode	Electron Inj. direction	Efficiency (= Ig/I)	Parallel write bit#／1mA	Issues	Oxide reliability	Cell (Name)
N-ch Cell	CHE	to FG	10^{-6}	~2	Page non-writable	No problem	ETOX etc
	SSI	to FG	10^{-3}	~2k	Complicated cell	Inj. time increase	SST
	Local-FN	to S/D	10^{-3}	~2k	B-t-B hole / SILC	Retention/R-dtb	DiNOR / AND
	Edge-FN	to FG	~1	~2M	High field / SILC	Retention/R-dtb	NAND
P-ch Cell	DAHE	to FG	10^{-3}	~2k	P/E bias design	?	?
	BTBT	to FG	10^{-2}	~20k	Electron Trap-up	Inj. time increase	P-ch DiNOR/ PMC[7]
	Edge-FN	to FG	10^{-2}	~20k	Electron Trap-up	Inj. time increase	P-ch DiNOR/ PMC[7]