Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 142-143

High-Performance EEPROMs Using N- and P-Channel Poly-Si TFTs with ECR N2O-Plasma Oxide

Nae-In Lee*, Jin-Woo Lee, Hyoung-Sub Kim*, and Chul-Hi Han

Department of Electrical Engineering, KAIST
373-1, Kusong-dong, Yusong-gu, Taejon, 305-701, Korea
Phone : +82-42-869-8044, Fax : +82-42-869-8530, E-mail : slee@cais.kaist.ac.kr
* Semiconductor R & D Center, Samsung Electronics Co. Ltd.

1. Introduction

Poly-Si TFT EEPROMs are very attractive for applications in LSI circuits and memories for image storage of portable handy terminals and digital still cameras [1], [2]. However, previously reported poly-Si TFT EEPROMs show poor performance and preliminary nonvolatile functions due to poor tunnel oxide [1]. To achieve high-performance poly-Si TFT EEPROMs, high quality thin tunnel oxide is greatly required. In our previous report, ECR N_2O-plasma oxide grown on poly-Si has a significantly low electron trapping rate and excellent charge-to-breakdown (Qbd) characteristics [3]. In this paper, we present for the first time high-performance poly-Si TFT EEPROMs using CMOS poly-Si TFTs with ECR N_2O-plasma oxide.

2. Experiments

Fig. 1 shows a schematic of the planar poly-Si TFT EEPROMs using n- and p-channel poly-Si TFTs with a common floating gate. The p-channel poly-Si TFT has a continuous inversion channel during programming and erasing because the potential of the floating gate is lower than that of the control gate. This leads to higher coupling ratio than twin poly-Si TFT EEPROMs [1]. To fabricate poly-Si TFTs, active a-Si film of 100nm thickness was deposited using SiH_4 gas and annealed at 600℃ for 48hours in N_2. Then, ECR N_2O-plasma oxide of 9.8nm thickness was prepared at 400℃, 1.4mtorr and 600W. After the floating gate electrode of 300nm was patterned, source and drain regions were formed by As and BF_2 ion implantation with a dose of 5×10^{15} cm^{-2} at 40keV, respectively. After contacts were opened, aluminum was deposited and patterned.

3. Results and Discussion

Fig. 2 shows the Weibull plots of Qbd for ECR N_2O-plasma oxide. ECR N_2O-plasma oxide has Qbd up to $10C/cm^2$, which is comparable to oxide thermally grown on crystalline silicon. From SIMS and XPS analysis, nitrogen atoms pile-up and form a nitrogen-rich layer near the oxide/poly-Si interface. The N(1s) peak was observed at a binding energy of 397.8eV, which means that there exist strong Si-N bonds which have much stronger endurance under electrical stressing than weak Si-O bonds [4].

Fig. 3 shows I_D-V_G transfer characteristics of poly-Si TFT EEPROMs after programming and erasing. The width and length of the NMOS TFT are 5㎛ and 5㎛, respectively. The devices were programmed and erased by applying 12.5V and -10V for 10ms to the control gate under $V_S=V_D=0V$, respectively. The threshold voltages were defined by $I_D=10nA\times(W/L)$ at $V_{DS}=0.5V$. The threshold voltages of the device are 1.3V and 5.3V after erasing and programming, respectively. The ON and OFF current ratio of both programmed and erased devices are about 10^7 at 0.5V drain bias, which is sufficient for EEPROM applications [5].

Fig.4 shows programming and erasing characteristics of poly-Si TFT EEPROMs. The programming and erasing were performed through F-N tunneling over the channel area by applying a positive and negative voltage to the control gate, respectively. The threshold voltage shifts of the programmed and erased devices are higher at the larger programming and erasing voltages and saturate within 1ms regardless of the programming and erasing voltages. The threshold voltage shifts of the programmed and erased devices are 3.87V at $V_P=12.5$ and -3.8V at $V_P=-10V$ for 10ms, respectively.

Fig. 5 shows endurance characteristics of the poly-Si TFT EEPROMs. The threshold voltage shifts are about 4V within 10^3 program and erase cycles. Although the threshold voltages of the erased devices increase after 10^3 program and erase cycles due to the electron trapping in the oxide, the poly-Si TFT EEPROMs have a large threshold voltage shift of 2.5V even after 1×10^5 program and erase cycles, which is attributed to the excellent Qbd up to $10C/cm^2$ of ECR N_2O-plasma oxide. This means that there is no endurance problem in poly-Si TFT EEPROMs.

4. Conclusions

High-performance EEPROMs using complementary poly-Si TFTs have been demonstrated. The fast programming and erasing were accomplished by F-N tunneling within 1ms regardless of programming and erasing voltages. Poly-Si TFT EEPROMs have threshold voltage shifts of about 4V between programmed and erased states, furthermore, a large threshold voltage shifts of 2.5V even after 1×10^5 program and erase cycles. It is attributed to the excellent Qbd up to $10C/cm^2$ of ECR N_2O-plasma oxide. We can directly realize LSI circuits and memories for image storage on the periphery of the display using CMOS poly-Si TFT EEPROM process.

References

1) M. Cao, T. Zhao, K. C. Saraswat, and J. D. Plummer : IEEE Trans. Electron Device Lett. **15** (1994) 304.
2) N. D. Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French : IEEE Trans. Electron Devices **43** (1996) 1930.
3) N. I. Lee, J. W. Lee, S. H. Hur, H. S. Kim, and C. H. Han : IEEE Trans. Electron Device Lett. **18** (1997) 486.
4) R. I. Hedge, P. J. Tobin, K. G. Reid, B. Maiti, and S. A. Ajuria : J. Appl. Phys. Lett. **66**, (1995) 2882.
5) S. Koyama : Symp. VLSI Tech. (1992) 44.

Acknowledgments

The authors would like to thank H. S. Yang, H. G. Kim, and C. Y. Cho from Samsung Electronics Co. for experimental assistance.

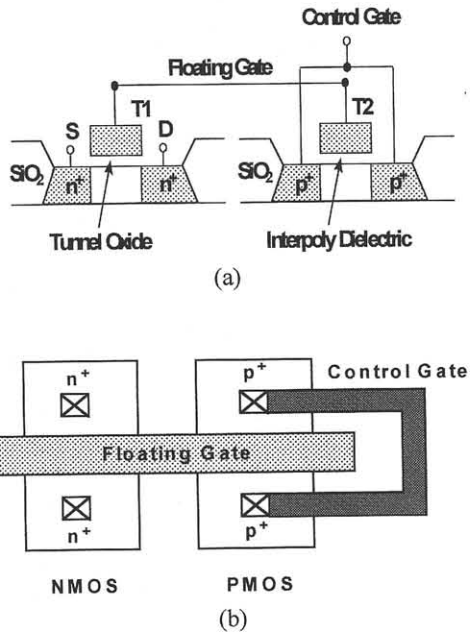

Fig. 1 Cross-sectional (a) and top view (b) of the poly-Si TFT EEPROMs using CMOS poly-Si TFTs with a common floating gate.

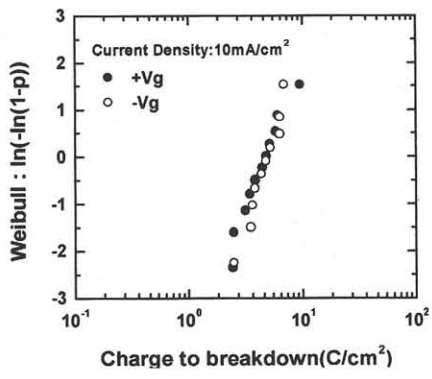

Fig. 2 Weibull plots of charge-to-breakdown of capacitors with ECR N_2O-plasma oxide under positive and negative constant current density of 10mA/cm^2.

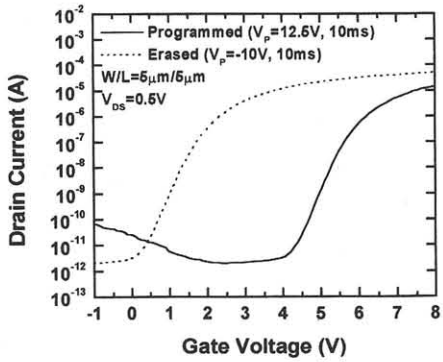

Fig. 3 I_D-V_G transfer characteristics of poly-Si TFT EEPROMs after programming and erasing.

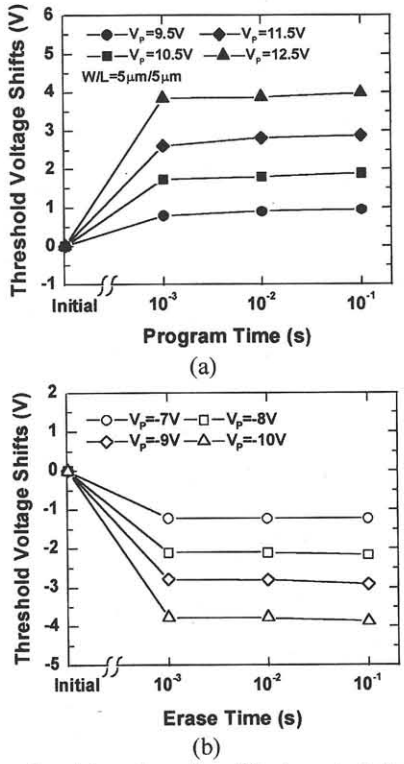

Fig. 4 Programming (a) and erasing (b) characteristics of poly-Si TFT EEPROMs. The programming and erasing were performed through F-N tunneling over the channel area.

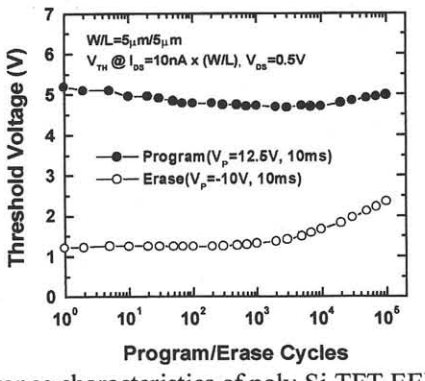

Fig. 5 Endurance characteristics of poly-Si TFT EEPROMs.