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Characteristics and Correlated Fluctuations of the Gate and Substrate Current after Oxide Soft-Breakdown

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1. Introduction

It is known for some time that ultra-thin oxide layers (< 5.5 nm) can breakdown in a soft way, i.e. without the lateral propagation of the breakdown spot due to thermal damage [1]-[3]. Most of the works on soft-breakdown (SBD) use capacitors where only the gate current can be monitored. In this study we use nMOSFETs to investigate the properties of the gate and the substrate current after SBD and to analyze the corresponding correlation.

2. Experimental

The devices used in this work are nMOSFETs with oxide thickness of 4.5 nm and with two different areas of 5 and 500 μm^2. The gate oxide was grown in wet ambient at 700 °C. The poly-Si gate was implanted with Phosphorus (dose $2x10^{14}$ cm^{-2}) at 30 keV.

3. Results and discussion

Fig. 1 shows the evolution of the gate and substrate current during a 6.5 V voltage stress. At the moment of the SBD, the jump in the substrate current is three decades, much higher than the gate current jump. As a consequence the increase of the substrate current can be used as a sensitive SBD detector

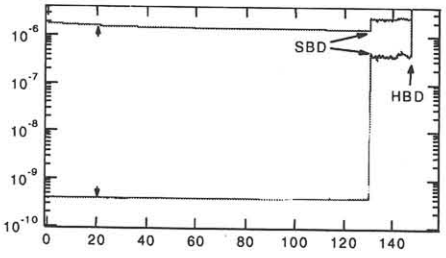

Fig. 1 Comparison between the gate and the substrate current jump at SBD moment during a 6.5 V gate voltage stress in a 500 μm^2 area nMOSFET.

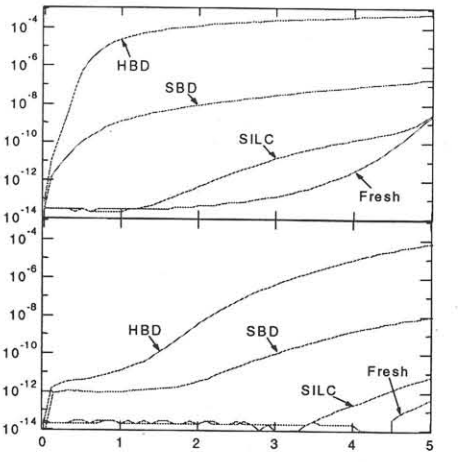

Fig. 2 Gate and substrate current vs gate voltage for different degradation stages in a 4.5 nm oxide thickness nMOSFET.

for nMOSFETs stressed with positive gate polarity. Fig.2 shows the gate and the substrate current as a function of the gate voltage for four oxide degradation stages. Notice that after SBD, not only the gate current, but also the substrate current increases in the whole voltage range. It consists out of a constant component at low voltage and a rising component at higher voltage. The rising part can be modeled empirically as a FN-current with a 1.1 eV barrier height.

It has been reported that after SBD the gate current shows RTS behavior [3]. RTS was easier to detect in the smaller samples. After SBD a 5 μm^2 area nMOSFET was stressed at different gate voltages, chosen to be sufficiently high to induce RTS fluctuations and sufficiently low to avoid further oxide degradation. The results of this series of measurements are reported in Fig. 3 and Fig. 4. Fig. 3 shows the evolution of the gate current for different gate bias. For each voltage, a clear two-level RTS was observed and the amplitude of the

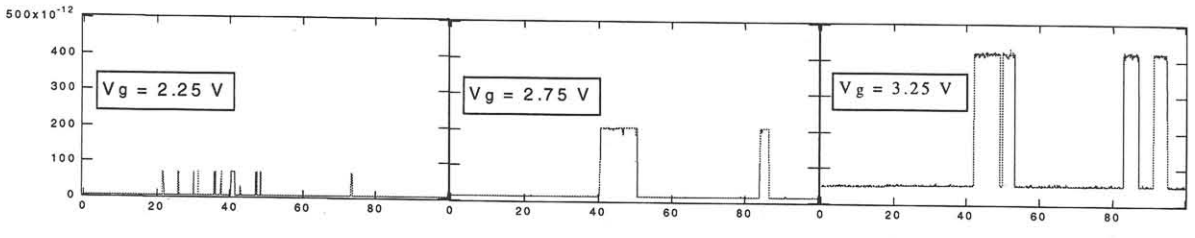

Fig. 3 Two level RTS in the gate current at different gate voltages after SBD in a 5 μm^2 area nMOSFET. The fluctuations amplitude increases with the applied voltage.

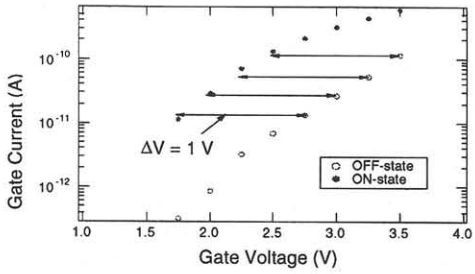

Fig. 4 The ON and the OFF state values of the gate current are shifted over a constant voltage interval.

fluctuations increases with the applied voltage. Fig.4 shows the ON and OFF state values of the currents for all measured gate voltages. It is found that the ON and OFF curves are shifted over a constant voltage interval. This explains the higher current fluctuations at higher voltages. The ON and OFF states can be explained by the capture and emission of a single electron on a slow oxide trap. The capture of an electron causes a shift of the local injection field by an amount $\Delta E = q/(\varepsilon A)$, where A is the area within which the electric field is significantly affected by the trapping [4]. Since two-level or multilevel RTS are always observed in the 5 μm^2 area nMOSFETs, from statistical considerations we assume that the traps causing RTS are part of the SBD path. As the gate current ratio between ON and OFF state was very high in this sample, it is concluded that the trap causing RTS was very close to the substrate. Therefore the area A is given by:

$$A = \frac{q}{\varepsilon \cdot \Delta E} = \frac{q \cdot t_{ox}}{\varepsilon \cdot \Delta V} \qquad (1)$$

where t_{ox} is the oxide thickness. For ΔV = 1 V and t_{ox}= 4.5 nm, the area of the SBD spot, A, is calculated to be $2x10^{-13}$ cm^2. In some sample it was possible to observe two independent but superimposed RTSs, as shown in Fig. 5. Notice that when the slower trap is in the ON state, the amplitude of the faster signal is higher, in agreement with the previous results. Finally we have investigated the correlation between the gate and the substrate current after SBD. For this purpose, we have plotted the gate current vs substrate current after SBD at high fields during the stress of Fig.1, as shown in Fig. 6, and at low fields during the RTS regime, as shown in Fig. 7. In the first case, it is

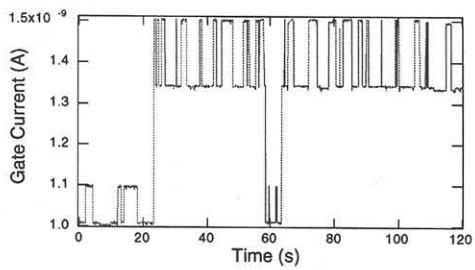

Fig. 5 Two RTSs superimposed upon each other at gate bias of 2.5 V.

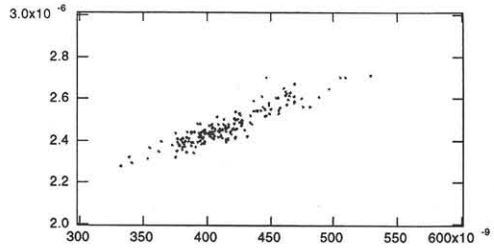

Fig. 6 Strong correlation between the gate and the substrate current after SBD during the stress of Fig.1.

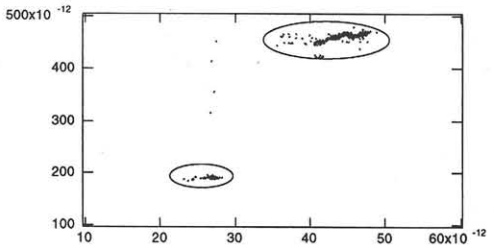

Fig. 7 Directly correlated RTSs in the gate and substrate current after SBD at 2 V gate bias.

evident that the two current noises are linearly correlated. In the second case, directly correlated RTSs are observed. An analogue result has been reported for the gate and the substrate current before breakdown [5]. These results imply that both currents must be generated at the same location and are influenced by the local electric field fluctuations.

4. Conclusions

It has been shown that the ON and the OFF state of the current through the oxide after soft-breakdown are shifted over a voltage interval. This observation can be explained by the capture-emission process of a single electron on an oxide trap. It has been observed that in nMOSFETs the oxide soft-breakdown is characterized by a huge increase of the substrate current for all positive gate voltages. A strong correlation has been found between the gate and the substrate current after soft-breakdown at low fields during the RTS regime and at high fields.

References

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