

Invited

Surface Preparation, Growth, and Interface Control of Ultrathin Gate Oxides

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1. Introduction

Given the ever increasing circuit densities required by next generation microprocessors, memories, and logic products such as DSPs, gate insulators with thickness less than 3 nm will soon be required. Recently, the use of 1.5 nm to 2.5 nm gate oxides in CMOS devices has been demonstrated [1-2]. However, considering that the length of Si-O bonds is approximately 0.16 nm, there will be only a few tenth monolayers of SiO within the thickness of the SiO₂. Therefore, thickness controllability and quality of ultrathin gate insulators will become a major issue for further technological development. To clarify these issues, we have been researching the fabrication and control of atomically flat Si surfaces prior to gate oxidation, growth of ultrathin gate insulators, the control of the MOS interfacial structure and interface traps, and ultrathin oxide thickness metrologies.

Some of our recent research results from the Texas Instruments Tsukuba Research & Development Center are summarized below.

2. Experimental results

i) A Si(100) wafer was made atomically flat by annealing in diluted hydrogen (H₂ 5%-He 95%) as low as 900 °C. The Si surface exhibited nearly periodic monoatomic steps. The surface was also oxidized to grow SiO₂ with a thickness of 3nm. The surface showed almost identical step and terrace structures prior to oxidation, which suggests that oxidation of Si occurs very conformally on Si(100) surfaces [3].

ii) Si was oxidized in an N₂O ambient. A wide process window was found where the thickness of the very thin N₂O oxide is approximately 4 nm independent of growth temperature between 870 to 1000 °C. This was correlated to the increase of incorporated nitrogen with the increase of temperatures [4].

iii) 3 nm thick dry oxides grown at a low temperature (650 °C) and annealed at a high temperature (850 °C) showed superior electrical stressing immunities to the oxides grown at a high temperature (850 °C). The MOS interfacial transition layers disappeared after the annealing as confirmed by Grazing Incident X-ray Reflection (GIXR) measurements. The control of the MOS interfacial density in these ultrathin gate oxides is a critical factor [5].

iv) A new method to measure MOS interface trap energy distribution was proposed for ultrathin (2-3 nm) oxide capacitors to which the usage of the conventional C-V measurement was difficult to apply due to a large tunneling leakage current. A layer of 3nm-thick Pt was formed on the ultrathin oxides to form a MOS structures, and a bias voltage was given between the Pt electrode and the Si substrate in an XPS vacuum chamber. The energy shift of Si2p peak from the Si substrate was measured as a function of the bias, from which the interface trap energy distribution was obtained [6].

vi) A new technique to accurately measure thicknesses of ultrathin SiO₂ using self-assembled-monolayer thin films which as a masking material to etch SiO₂ and a extremely accurate standard for AFM thickness calibration [7].

In addition, we have started a new project to measure two thickness distributions of oxide on Si surfaces.

3. Summary

These results indicate that the characteristics of ultrathin gate insulators with a thickness less than 3 nm are significantly influenced by the atomic structures on the Si surfaces prior to gate insulator growth, the density of interface traps, and the structure of the interfacial transition layer between SiO₂ and Si-substrate.

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