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Through-the-Gate Implanted (TGI) CMOS Technology with Advanced Shallow Trench Isolation

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1. Introduction

Through-the-Gate Implantation (TGI) of channel and well doping [1] can be favorably combined with n+/p+ gate implantation. This approach offers an additional degree of freedom to optimize dual-workfunction gates independently from ultra shallow S/D junctions which are needed for deep sub-µm CMOS. By using the same masks for each device type, no increase in process complexity occurs.

In this work, we present results on a novel through-the-gate implanted CMOS-STI technology utilizing N_{14} co-implantation to minimize gate cross-diffusion, also to improve narrow width characteristics and to suppress Boron penetration as well. Simultaneously, excellent short channel behavior and high drive currents are obtained with TGI CMOS.

2. Process Concept and Device Fabrication

The process starts with gate oxidation (4.6nm) followed by bottom-poly (200nm) and nitride deposition (Fig. 1). Isolation and active device regions are defined by anisotropic trench etch followed by a brief oxidation to create a small gate-bird's-beak at the trench edge to prevent parasitic corner leakage [2,3]. Subsequently the trench is filled with CVD oxide. Oxide planarization stops at the nitride layer. After nitride removal and sacrificial oxide growth, channel- and well-dopants are implanted through the bottom-poly. With the same masks, the respective n+ and p+ implantations into the poly are carried out. Optional, N_{14} is co-implanted into the bottom-poly. A brief high temperature anneal is applied to cure any implantation damage and to activate the implants. Subsequently the top-gate poly is deposited and both, top- and bottom-poly are structured using the regular gate mask. This step also removes redundant poly from active areas. Subsequent processing continues with source/drain formation, including shallow extensions with pockets. $TiSi_2$ salicidation and back-end metallization completes CMOS fabrication.

3. Electrical Results and Discussion

Fig. 2 summarizes the Vth (L) characteristics of TGI CMOS. The usual Vth roll-off is slightly over-compensated by pocket implantation. A small residual roll-up of 50mV and 70mV (L=10 to 0.15µm) remains for PMOS and NMOS, respectively. We obtain tight Vth spreads across the wafer despite implanting through gate poly. Co-implantation of N_{14} shifts the PMOS-Vth by -100mV, indicating efficient suppression of Boron penetration [4]. Besides minor change of oxide charges, the NMOS is virtually unaffected by N_{14} gate implantation. Excellent sub-Vth slopes (77- 79mV/dec) without 'STI-kink effect' and high saturation currents are obtained for NMOS and PMOS devices (Fig. 3). Consistent with this result, no mobility degradation is encountered by TGI when compared to conventionally implanted CMOS reference devices (Fig. 4) with identical Vth (PMOS). Small deviations (NMOS) are due to Vth differences. Also, no major deterioration of gate oxide reliability was noted for through-the-gate implanted CMOS, consistent with previous results [1].

Due to the absence of the parasitic corner device, EXTIGATE [2,3] STI is less sensitive to narrow channel effects (NCE). This enables us, for the first time, to examine the impact of Boron penetration (BP) in narrow STI-bounded PMOS structures with thin gate oxides. As evident from Fig. 5, BP is obviously size dependent. The 100mV Vth-shift vanishes gradually with decreasing channel widths towards 0.2µm and finally approaches the same Vth of N_{14} co-implanted devices. Without BP, (i.e. N_{14} implanted), the Vth is very uniform (<10mV) over the whole width range. Again, for NMOS devices N_{14} implantation has no drastic effect on Vth (Fig. 6).

The impact of N_{14} co-implantation on lateral impurity diffusion within n+/p+ gates was investigated by using MOSFETs connected to diffusion sources at varying distances. As shown in Fig. 7, Vth-shifts due to counter-doping effects are also reduced by N_{14} co-implantation. Since the presence of N_{14} is known to reduce the vertical diffusivity of Boron in poly [5], we assume that a similar effect retards the diffusion in the lateral direction.

In conclusion, this novel TGI CMOS technology provides a promising alternative for process and device integration towards future sub-0.1 µm CMOS ULSI.

Acknowledgments

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References

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[4] T. Kuroi et al., Symp. on VLSI Tech. p. 107 (1994)
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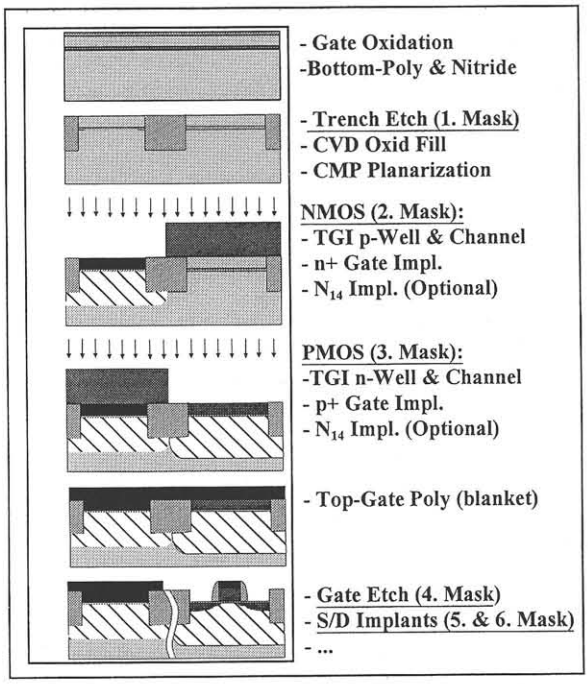

Fig. 1: Essential part of the through-the-gate implanted (TGI) CMOS technology with EXTIGATE [2,3] shallow trench isolation.

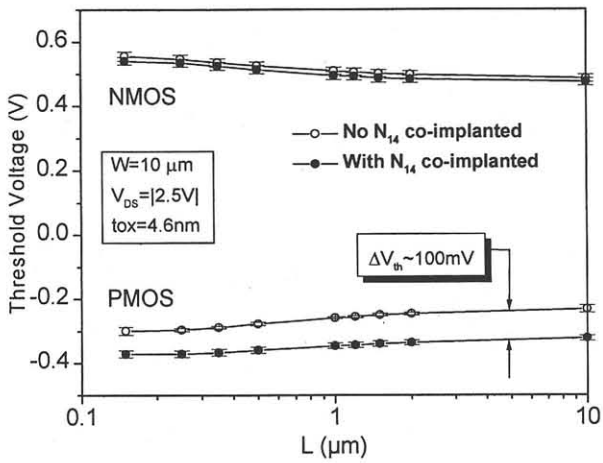

Fig. 2: Vth (L) characteristics of TGI CMOS with and w/o N_{14} co-implantation. Vth roll-up: 50mV (PMOS) and 70mV (NMOS). Error bars indicate Vth spread across the wafers.

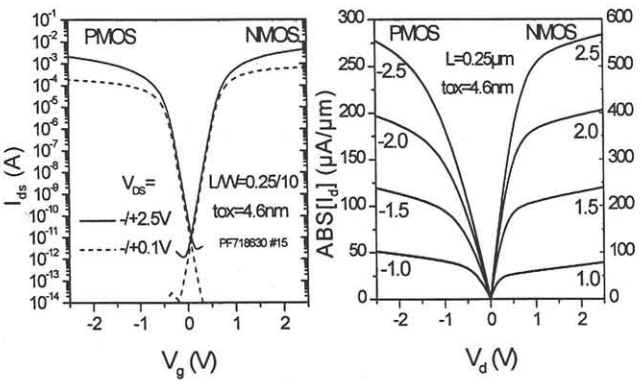

Fig. 3: I-V characteristics obtained by TGI CMOS devices with N_{14} co-implantation and EXTIGATE STI isolation.

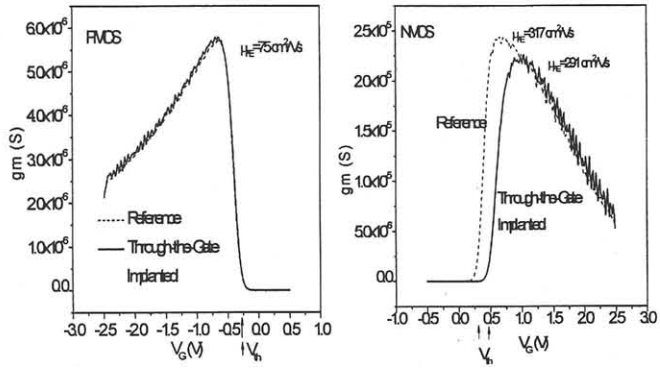

Fig. 4: No mobility loss despite TGI and N_{14} implantation.

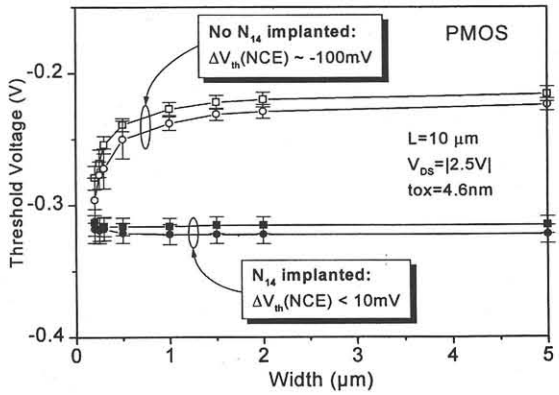

Fig. 5: N_{14} co-implantation substantially improves narrow channel effect (NCE) for PMOS devices (2 wafers each split).

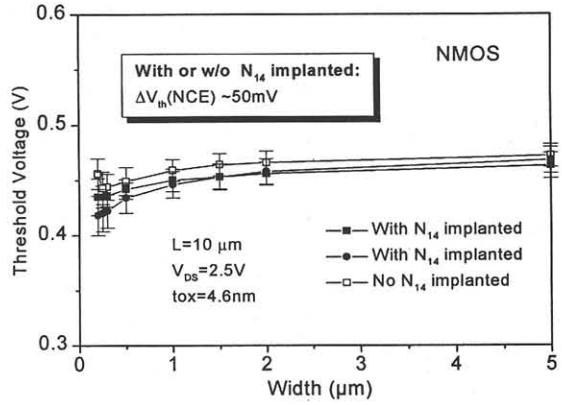

Fig. 6: Narrow channel behavior of NMOS devices is not significantly affected by N_{14} co-implantation

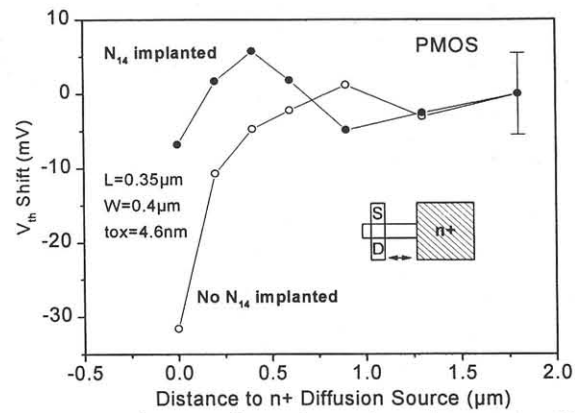

Fig. 7: Counter-doping effects due to lateral impurity diffusion between n+/p+ gates are reduced by N_{14} implantation.