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Improved Ti SALICIDE Technology Using High Dose Ge Pre-Amorphization for 0.10um CMOS and Beyond

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Abstract

Improved Ti SALICIDE technology using high dose pre-amorphization implantation(PAI) is developed. Low sheet resistance down to 0.10μm gate length without degrading the MOSFET characteristics is successfully demonstrated by Ge PAI. In addition, the advantage of Ge PAI over conventional As PAI is confirmed.

Introduction

SALICIDE (self-aligned silicide) technology has been applied for CMOS LSI since it can achieve both low sheet resistance(Rs) of gate electrodes and reduced source/drain parasitic resistance. Among several silicides, $TiSi_2$ exhibits superior characteristics such as low resistivity, and good thermal stability. Moreover, strong deoxidizing nature of Ti is beneficial for process integration since it is relatively insensitive to surface condition prior to silicidation.

Despite these advantages of $TiSi_2$, it becomes unclear whether it can be applied to 0.15μm CMOS and beyond because of Rs increase in narrow lines(narrow line effect). Its mechanism is explained that transformation of $TiSi_2$ from C49 to low resistive C54 phase is retarded in narrow lines due to the decrease of nucleation sites which are considered the triple points of C49 grain boundaries. Recently As or Ge PAI before silicide formation is found effective to suppress the narrow line effect with 0.1μm gate length[1,2]. However, the degradation of MOSFETs drive current is observed and its mechanism is not fully clarified yet.

Thus it becomes important to characterize PAI effects on device performance in detail in order to apply it to smaller dimension CMOS technology. In this paper, we have studied the effect of As and Ge PAI on Rs of fine lines and MOSFETs characteristics, and clarified that Ge PAI with high dose up to $1x10^{15}cm^{-2}$ is eminently suitable for 0.10μm CMOS generation and beyond.

Experiments

In this study, CMOSFETs with gate length down to 0.06μm were fabricated based on the 0.15μm CMOS technology. Figure 1 shows the process sequences of PAI Ti-SALICIDE technology. After the shallow extensions were made, the sidewall formation was followed by simultaneous doping of diffusions and gate electrodes. After an activation rapid thermal annealing(RTA), the surface of diffusions and poly-silicon gates was pre-amorphized by Ge or As implantation(PAI), where the dose was varied from 1×10^{14} to 1×10^{15} cm^{-2} while changing the energy from 15 keV to 50 keV. Ti/TiN deposition were followed by two step RTA process. Silicidation(1st RTA) was performed at 700℃. After metal strip, phase transformation of $TiSi_2$(2nd RTA)was carried out at 800℃. Fabricated samples were electrically and/or physically evaluated with emphasis on the PAI dose and species(As or Ge) dependence. For part of samples, only 1st RTA was carried out at 600℃ and was characterized to investigate the PAI effect on silicide growth.

Effect of high dose PAI on $TiSi_2$ sheet resistance

Rs as a function of gate length is shown in Fig.2 (a) and (b) for Ge and As PAI, respectively. With PAI dose of $10^{15}cm^{-2}$, the improved uniformity of Rs down to 0.1μm gate length is obtained both for Ge and As PAI. In contrast the increase in Rs around 0.17μm is observed when PAI dose is $10^{14}cm^{-2}$. This PAI dose dependence of Rs is explained by the enhanced C49 to C54 transformation due to the increased density of nucleation sites by PAI. A similar suppression of Rs increase down to 0.18μm line width is obtained for the diffusion layers as shown in Fig.2 (c).

To examine the PAI effect on silicide growth, gate length dependence of Rs after 600℃ 1st RTA is evaluated as shown in Fig.3(a), where Rs reflects the silicide thickness directly because $TiSi_2$ is all C49 phase with this low temperature RTA. With high dose Ge PAI, the increase of Rs in fine lines is suppressed. The formed silicide-thickness vs. PAI dose is also evaluated by TEM observation of 0.12μm gate electrodes as shown in Fid.3(b) and (c). It is confirmed that the high dose PAI improves the silicide growth rate by factor of two and is truly effective to achieve low Rs of gate electrodes and diffusions.

Species dependence of PAI on MOSFET performance

As mentioned above, high dose PAI improves the silicidation process. However, such high dose PAI could cause device characteristics degradation. The strong PAI dose dependence of parasitic resistance(Rpara) of pMOSFETs is observed for As PAI as shown in Fig.4(a), while no degradation is found with Ge PAI. This increase in Rpara with As high dose PAI process is resulting from the increase in silicide-silicon contact resistance as shown in Fig.4(b). High contact resistance of 120 Ω μm^2 by As PAI with the dose of $1x10^{15}cm^{-2}$ indicates that it is caused by the compensation with implanted As near the silicide/ p^+silicon interface which is expected from the doping profile of p^+ junction as shown in Fig. 5. Fig. 5 also suggests such degradation due to the impurity compensation could be prevented by lowering the PAI energy. However, the improvement of Rs by As PAI disappears at lower energy, as the energy dependence on Rs of 0.15 μm gate is shown in Fig. 6. Thus, Ge is superior to As for high dose PAI process because the former causes no performance degradation due to its electrical neutrality.

Conclusion

Utilizing high dose Ge PAI, Ti SALICIDE processes can be applied to 0.1μm CMOS devices and beyond. High growth rate of silicidation and low sheet resistance at narrow lines are achieved by high dose PAI. Ge high dose PAI is superior to As PAI because of no influence on the device characteristics due to its electrical neutrality.

References

[1]J. A. Kittl, et al., VLSI Tech. Dig., p.14 (1996).
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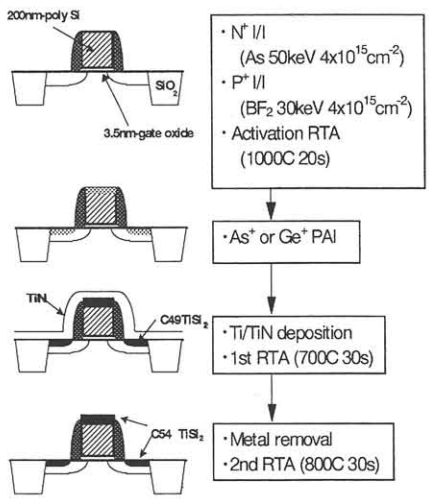
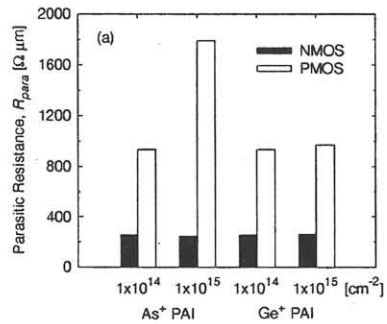


Fig. 1. Schematic cross section of Ti SALICIDE process with PAI.



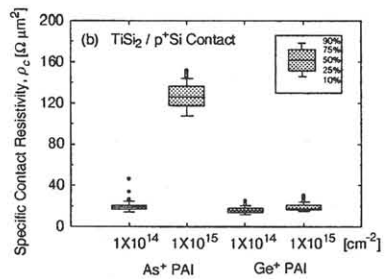


Fig. 4(a). Dependence of parasitic resistance (R_{para}) on PAI conditions. R_{para} of pMOSFET with high dose As PAI is two times higher than that of other PAI conditions.

(b). Dependence of $TiSi_2/p^+$-silicon specific contact resistivity (ρ_c) on PAI conditions. ρ_c with high dose As PAI is 6 times as large as that of other PAI conditions.

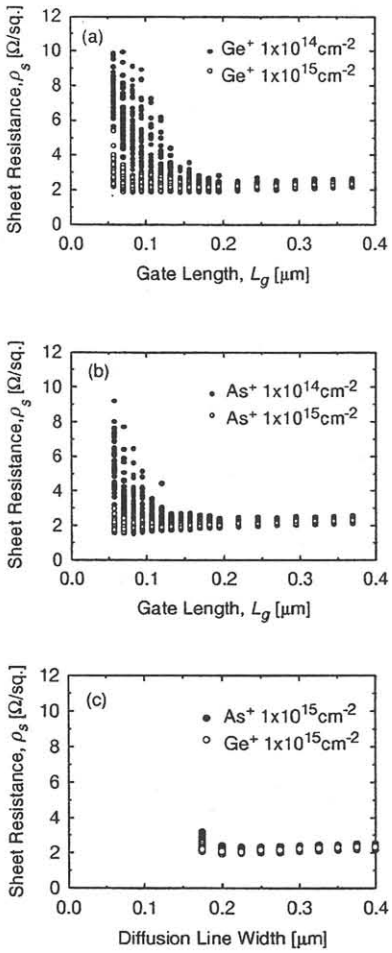
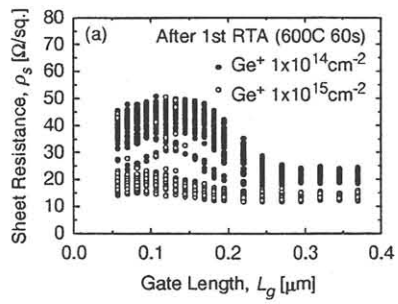


Fig. 2. Dependence of $TiSi_2$ ρ_s after 2nd RTA on PAI conditions: (a) for gate electrodes with Ge PAI; (b) for gate electrodes with As PAI; (c) for diffusion layers with high dose PAI.



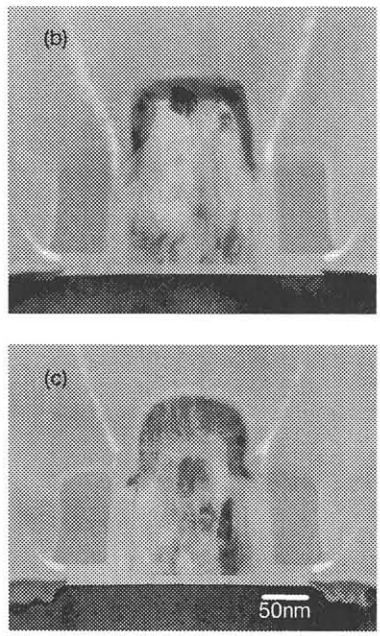


Fig. 3. PAI effects on silicidation: (a) ρ_s of $TiSi_2$/*C49* with Ge PAI dose as a parameter. Cross sectional TEM images of 0.12 μm gate electrodes with low dose (b) and high dose(c) Ge PAI.

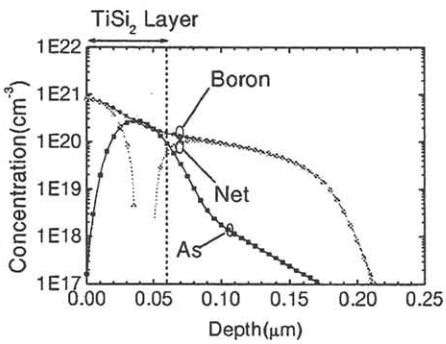


Fig. 5. Depth profile of B and As on p^+ diffusion layer. Net concentration of acceptor decreases near the interface of $TiSi_2$/silicon due to the impurity compensation.

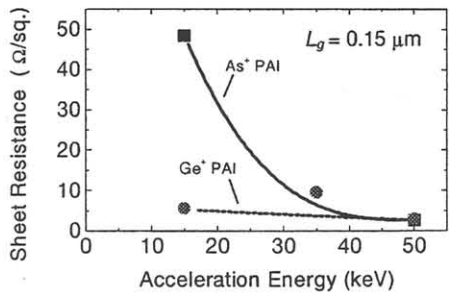


Fig. 6. Dependence of $TiSi_2$ ρ_s on PAI acceleration energy. Both doses are equal to $1x10^{15}$ cm^{-2}. With decreasing acceleration energy, PAI effect disappeared in As PAI , while not in Ge PAI.