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Improvement of Ultra-Thin 3.3nm Thick Oxide for Co-Salicide Process Using NF3 Annealed Poly-Si Gate

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1. Introduction

Reliability of the gate oxide becomes more and more stringent than ever before as the device size scales down to the deep-submicron era. Current leakage will become a critical factor for the scaled-down of the gate oxide thickness for the deep submicron device, especially for the low field leakage current before the F-N tunneling. It has reported that the reliability of MOS capacitors can be improved by introducing minute amounts of fluorine in thermal oxide [1]. On the other hand, using nitrogen implant through a poly-Si gate MOS structure to improve thin-gate characteristics has been proposed [2]. In this paper, we demonstrated, for the first time, a novel technique to incorporate both F and N to improve the gate oxide integrity. The process we proposed is the NF_3 annealed poly-Si gate after the growth of the ultra-thin gate oxide. On the other hand, reduction of gate, source and drain parasitic resistance without a junction leakage problem is a key issue in deep-submicron CMOS devices [3,4]. The conventional Ti-salicide process does not lead to significant junction leakage, but it is difficult to achieve a low gate resistance in narrow width [3,4]. The Co-salicide process can successfully reduce the gate resistance and becomes the main stream technology for next generations. However, the Co-salicide process has a junction leakage problem, and there has been no much report on its effect on the ultra-thin oxide integrity. Consequently, the capacitor with ultra-thin gate oxide, 3.3 nm, with Co-salicide process will be also investigated by using the NF_3 annealing.

2.Experimental

The initial wafer is (100)-oriented p-type silicon wafer. The gate oxide with thickness of 3.3 nm was grown in diluted O_2 gas (N_2:O_2=10:1) at 900°C. Then the poly-Si film with 300 nm-thick was deposited, followed by annealing in diluted NF_3 gas at 600°C for 5-20 minutes. Then samples were split into two parts. One is conventional structure (Al/poly-Si/SiO_2/Si) and the other is Co-salicide structure ($CoSi_2$/poly-Si/SiO_2/Si). The thickness of Al film is 500 nm, while 50 nm for Co-film. A two-step annealing process was used for this Co-self-aligned silicide (Co-salicide) formation.

3.Results and Discussions

The characteristics of the ultra-thin oxide in terms of current vs. electrical field, I-E, were measured. The I-E curves of Al/Poly-Si/SiO_2/Si samples with gate oxide thickness about 3.3 nm for various annealing times are shown in Fig.1. Quantum oscillations were observed in these curves. It is clear that leakage current at low field of the NF_3-annealed sample is smaller than that of conventional sample. The breakdown field of NF_3-annealed sample is also higher than that of the conventional sample (Fig.2). This is suggested due to the F and N incorporation from NF_3 annealing resulting stronger Si-F and Si-N bonds. These bonds can fill a lot of dangling and/or weak bonds such as Si-H or Si-OH at SiO_2/Si interface. The distribution of leakage current at 2 V was shown in Fig.3. It is found that the leakage current of oxide with NF_3 annealing is significantly reduced. It is suggested that both N and F species can simultaneously neutralize the dangling bonds in the oxide. We believe the leakage paths, dominated by assisting of interface trap, can be effectively suppressed by the N and F incorporation at the interface using NF_3 annealing. To verify this point, secondary ion mass spectroscopy (SIMS) analysis was performed to identify the interface species. As shown in Fig.4, SIMS profiles show indeed a pile-up of N and F at the SiO_2/Si interface of the sample annealed in NF_3 for 10 minutes. From these results, we found the optimized condition for NF_3-annealed poly-Si gate is 10 minutes. Fig.5 shows the I-E curves of $CoSi_2$/poly-Si/SiO_2/Si samples with oxide thickness of 3.3 nm. It also had a voltage shift between the conventional samples and NF_3-annealed samples. In Fig.6, the breakdown field of NF_3-annealed sample shows a higher value than that of the conventional sample. The distribution of leakage current at 2V was shown in Fig.7. The leakage current distribution of NF_3-annealed sample exhibits almost one order of magnitude smaller than that of the control. The optimized condition of NF_3-annealed $CoSi_2$/poly-Si/SiO_2/Si samples is also 10 minutes. Fig.8 shows the charge-to-breakdown, Qbd, distribution of Co-salicide with different NF_3-annealed time. NF_3-annealed sample shows an improved Qbd than that of control sample.

4.Conclusion

NF3-annealed poly-Si gate has been demonstrated to improve the integrity of the ultra-thin 3.3 nm oxide with Al or Co-salicide electrode in terms of leakage, breakdown field, and charge-to-breakdown. This process is very promising for future deep-submicron device fabrications.

References

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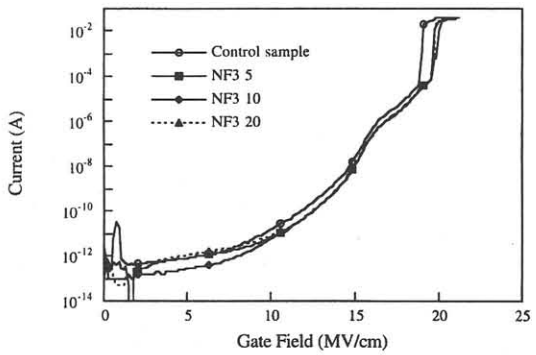

Fig.1 I-E curves of Al samples with different NF3 annealing time.

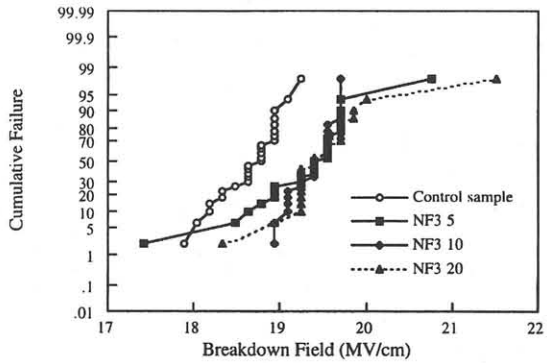

Fig.2 Breakdown field of Al samples with different NF3 annealing time.

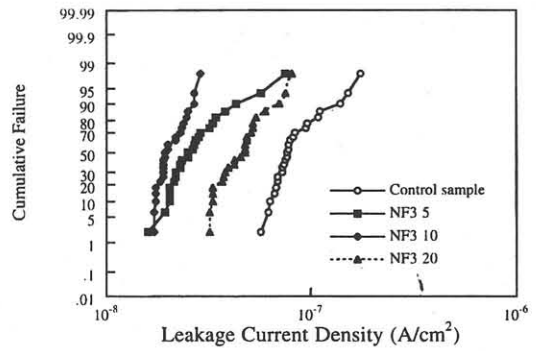

Fig.3 Leakage current of Al samples with different NF3 annealing time.

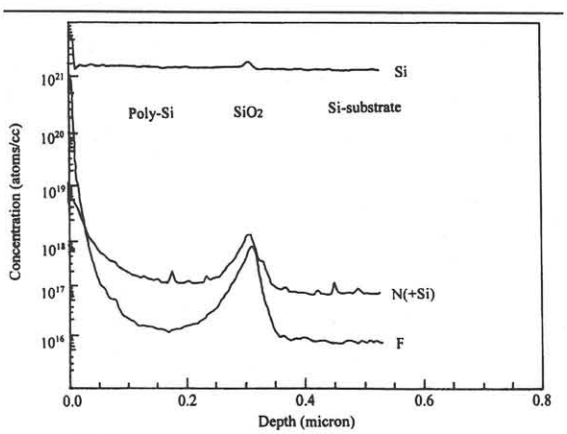

Fig.4 The SIMS profiles of sample annealed by NF3. It is found that F and N pile up at the SiO2/Si interface.

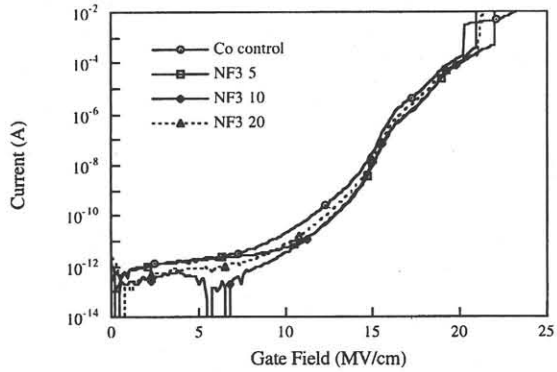

Fig.5 I-E curves of the Co-salicide sample with different NF3 annealing time.

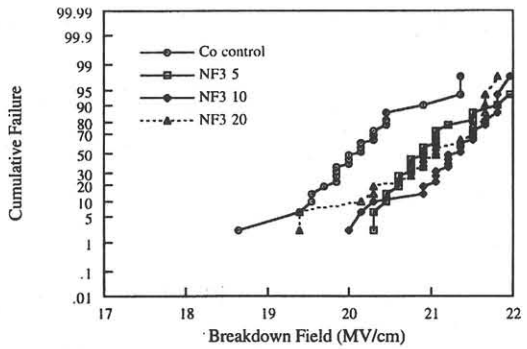

Fig.6 Breakdown of the Co-salicide with different NF3 annealing time.

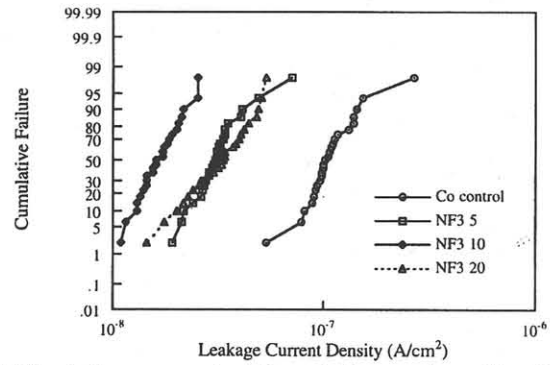

Fig.7 The leakage current of Co-salicide samples with different NF3 annealing time.

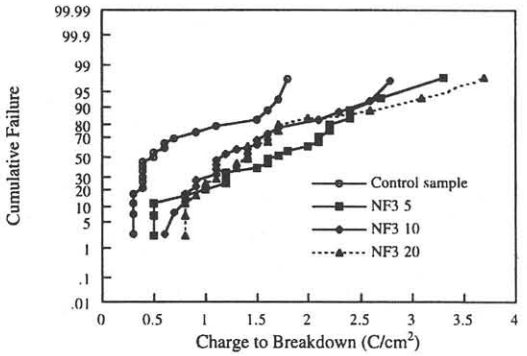

Fig.8 The charge-to-breakdown distribution of Co-sample with different NF3 annealing time.