Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 166-167

Bandgap Engineering for the Suppression of the Short Channel Effect of sub-0.1um p-channel MOSFETs

A. Nishiyama, K. Matsuzawa and S. Takagi
Advanced Semiconductor Devices Research Laboratories, R&D Center, Toshiba Corporation
Phone:+81-45-770-3667, Fax: +81-45-770-3578 e-mail:a-nishiyama@amc.toshiba.co.jp
8 Shinsugita-cho, Isogo-ku, Yokohama,235-8522 JAPAN

Abstract

A suppression of the short channel effect with the SiGe source/drain structure is proposed and quantitatively calculated. The drain induced barrier lowering (DIBL) and the charge sharing is suppressed with the valence band discontinuity at the SiGe/Si interface. In order to take advantage of this structure, it is necessary to locate the interface at the pn junction or inside the channel region.

1.Introduction

The short channel effect is problematic especially for sub-0.1μm p-MOSFETs due to the relatively deep source/drain junctions. This effect comes from the charge sharing between the source/drain and the channel region as well as the drain induced barrier lowering(DIBL). The increase of the channel doping for the suppression of these phenomena leads to the degradation of the carrier mobility. Therefore, we propose a bandgap engineering method in this paper: As the p^+SiGe/n-Si interface forms a large valence band discontinuity, ΔEv[1], the charge sharing can be suppressed due to the narrowing of the depletion layer widths by the built-in potential reduction(Fig1(a)). For MOSFETs with very short channels, SiGe source/drain structure can retain a high potential barrier for holes which otherwise is lowered with a high drain voltage by DIBL(Fig.1(b)). The SiGe source/drain structure has been proposed in order to suppress the floating body effect of SOI devices[2] so far, however the bandgap engineering for the short channel effect suppression is investigated here at the first time .

2.Simulation

A device simulator(DIAMOND), in which physical parameters of SiGe such as bandgap, carrier mobilities and dielectric constant are implemented, was used in this analysis. The simulated structure is depicted in Fig.2: The gate oxide thickness is 3nm and the gate width is 1μm. The gate electrode is made of p^+-polysilicon and the substrate doping concentration is uniformly $1 \times 10^{18}cm^{-3}$. The source/drain layers have rectangular shapes with the junction depth of 50nm in which the impurity concentration is uniformly $1 \times 10^{20}cm^{-3}$. The entire source/drain region is made of SiGe, except in the case of the simulation shown in Figs. 5 and 6. The Ge concentration of 30% (ΔEv:0.22eV) is used except in the case of Fig.8 because it is the highest concentration for the 50nm SiGe layers which can be formed without threading dislocations[1].

3.Result and Discussion

The comparison of the Id-Vg characteristics for 50nm p-channel MOSFETs(Fig.3) shows that the DIBL is suppressed dramatically with the SiGe source/drain structure as expected. Figure 4 shows the hole current distribution with the drain voltage of -1V and the gate voltage of 0.9V for the devices shown in Fig.3. The hole current which flows into the channel region away from the gate electrode is suppressed for the SiGe structure. The Id-Vg characteristics when the SiGe layer is located only at the source region, only at the drain region or at both regions(Fig.5) shows that the SiGe source structure is much more effective than the SiGe drain structure. This confirms that the main principle of the suppression of the DIBL is a large potential barrier for holes retained by the valence band discontinuity at the source pn junction even with a high drain voltage. Id-Vg characteristics when the SiGe/Si interface is located inside or outside the channel region(Fig.6(a)) shows that when the interface is located outside the channel region, the suppression effect is not observed. This is because the valence band discontinuity is transformed to the conduction band discontinuity inside the source/drain region and does not work as the barrier for holes(Fig.6(b)). When the interface is located inside the channel region, the suppression effect is retained as in the case in which the interface is located at the pn junction.

The threshold voltage Vth and the subthreshold swing were simulated as a function of the gate length Lg(Fig.7). The L_{min} defined with the 10% decrease in Vth was reduced from 100nm to 80nm. Figure 8 shows the ΔEv dependence of Vth and the drain current drive at the gate voltage of Vth+1V for 80nm p-channel MOSFETs. The decrease in Vth is suppressed as the ΔEv increases. The current drive decreases presumably due to the presence of the energy barrier at the source/channel pn junction, but the decrease is less than 10% even when ΔEv is as large as 0.22eV. Finally, it should be mentioned that this SiGe structure is not very effective for n-channel MOSFETs because of the small discontinuity of the conduction band [1].

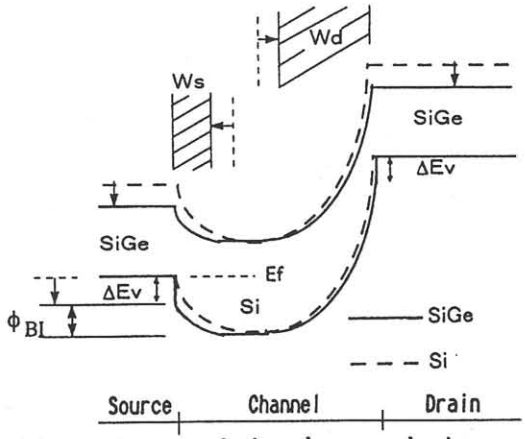
4.Conclusion

The bandgap engineering for the suppression of the short channel effect is proposed. This gives another technique for the reduction of the device dimension in the future.

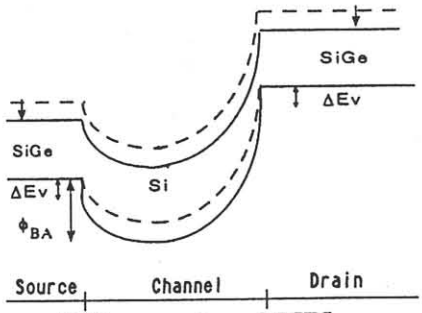
References

[1] R.People, IEEE J.Quantum Electron., QE22(1986), 1696.

[2] M.Yoshimi et al., Technical Digest of IEDM 1994, 429.



(a)Suppression of the charge sharing



(b)Suppression of DIBL source/drain structure

Fig.1: Bandgap engineering with the SiGe

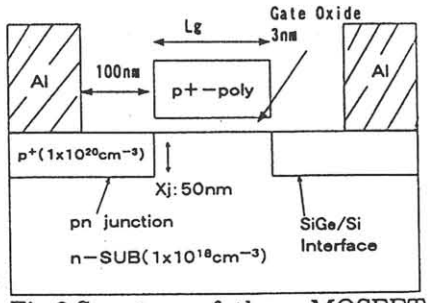


Fig.2:Structure of the p-MOSFET for this simulation.(Vs=Vsub=0V)

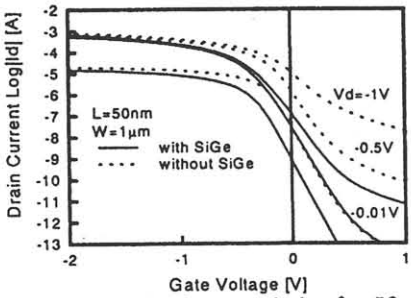


Fig.3:Id-Vg characteristics for 50nm p-channel MOSFETs. The drain voltages are -1, -0.5 and -0.01V from the top to the bottom for both cases.

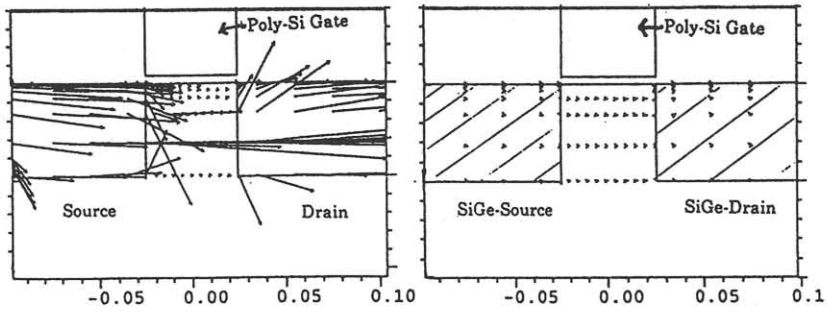


Fig4: Hole current flow distribution with the gate voltage and the drain voltage of 0.9V and -1V.

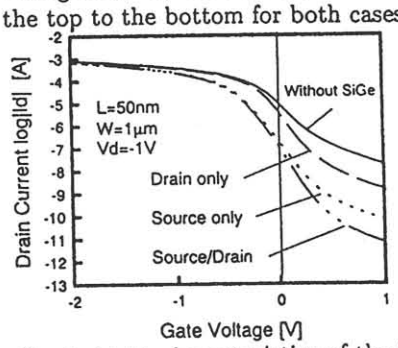
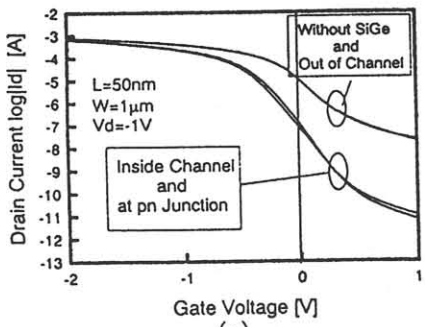


Fig.5: Id-Vg characteristics of the SiGe structure when the SiGe is located at the source region, at the drain region or at the both region.



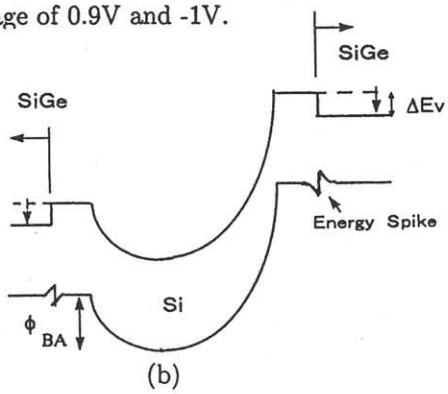
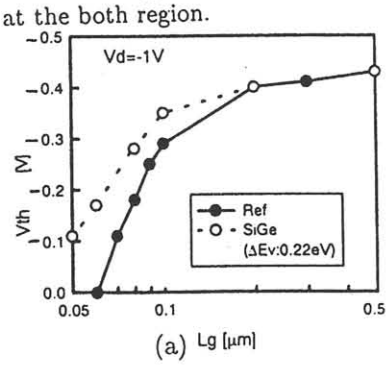


Fig.6:(a) Id-Vg characteristics of the SiGe structure when the SiGe/Si interface is located inside and outside the channel region.(b)Band diagram when SiGe/Si interface is located outside the channel region.



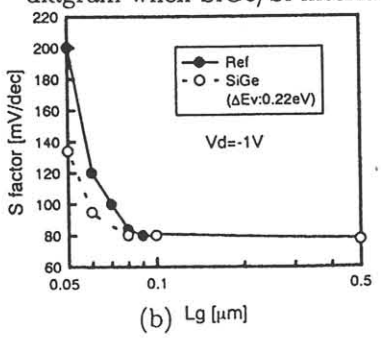


Fig.7(a) The threshold voltage Vth and (b)the subthreshold swing calculated as a function of Lg. The threshold voltage is defined as the gate voltage with the drain current of $0.1\mu A/\mu m$.

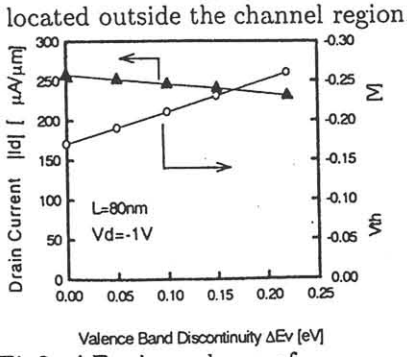


Fig8: ΔEv dependence of the threshold voltage the drain current for the gate voltage of Vth +1V.