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Silicon-on-Insulator Material for Deep Submission Technologies

W.P.Maszara

SEMATECH, Austin, TX and AMD, Sunnyvale, CA 94088, USA
Phone (408)749-3781, e-mail: witek.maszara@amd.com

1. Introduction.

Recent demonstration of fully functional high density, high performance circuits on SOI substrate - 1Gb DRAM by Hundai and 4Mb SRAM by IBM - vividly illustrates the dramatic improvement of the quality of SOI material.

Three categories of SOI wafers are currently in production: SIMOX, Unibond and ELTRAN. SIMOX is realized by implantation of high dose of oxygen (4-18e17 cm^{-2}) and high temperature annealing (~1350°C). Unibond and ELTRAN utilize wafer-bonding technique. In ELTRAN material the final thickness of the SOI film is determined by selective etching of buried porous Si layer, in Unibond it is an exfoliation of the top wafer by the buried layer of implanted hydrogen. The final product has Si and buried oxide (BOX) layers typically about 200 nm thick each, with the thicknesses varying within less than 10 nm across a 200 mm wafer. In this paper we will focus on the SOI material suitable for mainstream CMOS applications and issues related to its utilization.

SOI material has a unique set of peculiarities. Full understanding of their role in circuit design, performance, manufacturability and reliability will determine the acceptance of this material as a mainstream alternative, or, ultimately a material of choice for the future semiconductor industry. These SOI-specific features are:

- floating-body effects, both static and dynamic, caused by lack of low resistance path between substrate and MOSFET's body,
- partially or fully depleted operation of MOSFETs, controlled by thickness and doping of the SOI layer,
- poorer heat dissipation from junctions due to buried oxide's ~100 times lower thermal conductivity than silicon's.

While numerous high performance and lower density bipolar circuits, formed in thicker (>2 μm) SOI have been demonstrated and successfully entered commercial market several years ago, few mainstream products have been offered to the customers so far (gate array from Mitsubishi; PLL – Sharp; 0.5V wrist watch and wrist PC chips - Seico). Designing for proper handling of floating body effects and cost of the wafers appear to be the primary issues to determine the major entry of CMOS circuits into the market. It is expected that substantial gains in speed and savings in power at low voltages (<1.5 V) will be the main motivation for introduction of SOI into the mass-production CMOS market.

2. Material.

We have developed comprehensive, manufacturing oriented material characterization procedures to monitor SOI quality and have evaluated and compiled data on over 1500 wafers (200 mm) from all viable sources in the world.

All "generic" features of the 200 mm SOI wafers are quite mature and are comparable to bulk wafers: bow and warp, local flatness (STIR), surface contamination, surface roughness, edge exclusion. SOI-specific wafer parameters are all related to the structure of its two films. These are the thickness and thickness uniformity of both BOX and SOI, and the films' characteristic defects. Excellent SOI and BOX film thickness uniformity can be achieved by all three technologies. An across-wafer 6σ thickness uniformity illustrated in Fig.1 is around or below 10 nm for most products. A major yield-killer defects are those found in SOI film and referred to as HF-defects. We have found that in a mature material the dominant source of those are small pits (COPs) originating from the starting bulk material. Their density is similar to that found in CZ bulk material (~0.1/cm^2). HF defect density improved dramatically in the last two years, dropping over two orders of magnitude (Fig.2). Threading dislocations in SOI film are not known to pose a performance or reliability risk in CMOS devices on SOI. Our investigation of experimental low dose SIMOX material showed no impact of dislocations ranging in density from 1e4 to 1e7 cm^{-2} on gate oxide integrity. 65 A thick gate oxide integrity shows that all but standard dose SIMOX substrate is comparable to that of control CZ bulk material (Fig.3).

Table 1 shows comparison of SIA's National Roadmap for Semiconductors list of basic wafer parameter needs for the 0.25 and 0.18 μm technology nodes with the parameters of SOI wafers available on the market today. The comparison clearly indicates that the SOI material is well poised to meet the quality demands of high performance circuits of near future.

3. Processing issues.

Processing of SOI material requires recognition of some of its unique features such as its different optical properties. This would require adjustments to the metrology tools, including film thickness measurements, defect detection and analysis tools. Processing tools such as litho exposure tools and RTP may also needs some adjustments due to different SOI wafer reflectivity and emissivity respectively, but the adjustments, if any would be minor. The presence of buried oxide mandates minor redesigns of doping and isolation processes.

4. Availability.

Wafer suppliers' expectations, supported by significant investments to increase their production capacity, indicate that the availability of SOI material will rapidly increase to about 2 million 200 mm wafers a year in the year 2001. Their collective projections suggest that ~70% of the SOI material on the market in the year 2001 will be made by wafer bonding techniques and that the price of a 200 mm wafer in the year 2001 is expected to be about 3 times higher than that of a prime quality bulk wafer.

5. Summary.

Overall, it appears that today's SOI material largely delivers the desirable level of performance. Significantly improved over the last couple of years, the material, however, needs sustainable consistency of its parameters. The remaining starting material issues facing large scale, high performance circuit production are price and volume availability, rather than its quality. To remain an attractive alternative to the bulk silicon market, SOI wafer manufacturers will soon need also to concentrate on scaling up to the 300 mm wafer production. First 300 mm wafers in SIMOX and Unibond technologies have been recently demonstrated.

Table 1. Comparison of National Technology Roadmap for Semiconductors needs for substrate parameters and benchmarking data for SIMOX, Unibond and ELTRAN material.

Property	NTRS range for 0.18/0.25 μm	Material type		
		SIMOX (Ibis, Nipp.Steel, Komatsu)	Unibond (Soitec)	ELTRAN (Canon)
SOI film thickness uniformity, 6σ [Å]	50 - 200	yes	yes	yes
BOX film thickness uniformity, 6σ [Å]	200	yes	yes	yes
Surface roughness, Ra (1x1μm area) [Å]	1 – 1.5	yes (ex. Std. dose)	yes	yes
Surface metals [at./cm^2]	<2.5e10	yes	yes	yes
Site flatness, 25x25 mm [μm]	0.2 – 0.3	yes	yes	yes
BOX defects [1/cm^2]	0.09 – 0.12	0.1 - 7	yes	no data
HF defects [1/cm^2]	0.11 – 0.14	yes	yes	yes
Secco defects [1/cm^2]	4 – 5e4	yes (ex. Std. dose)	yes	yes