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Extremely Low Si Etching (<1nm) during Hydrogen Annealing of Silicon-on-Insulator

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1. Introduction

Gate oxide integrity is strongly affected by surface micro roughness, so that polishing is generally applied as the final treatment for fabrication processes of the silicon-on-insulator (SOI) wafers in spite of the SOI thickness reduction. Lately, hydrogen annealing was originated to smooth the SOI surface[1] which were rougher than that of bulk Si wafers and traced by several researchers[2-6]. In principle, hydrogen annealing hardly etch off Si films, however, various rates of etching Si were reported[1,2,7,8]. In this paper, Si etching during hydrogen annealing of SOI is investigated, and the extremely low Si etching less than 1 nm was achieved for the first time.

2. Experimental

SOI wafers are beneficial to evaluate the Si etching because the SOI thickness can be easily measured by a photoreflective method with accuracy in the order of 10^{-1} nm. It is superior to step height measurement[7], in which the etched thickness of Si is measured at the edge of a SiO_2 masking film on Si. We utilize ELTRAN[9-11] (epitaxial layer transfer) SOI wafers, in which epitaxial layers on porous Si are transferred onto handle wafers by bonding and etching back of porous Si. The surface after etching off the porous Si is smoothed by hydrogen annealing in advance to eliminate the effects of the surface roughness.

3. Results and Discussions

At first, hydrogen annealing was done in a barrel type reactor designed for epitaxial growth. Hydrogen gas flew parallel to the wafer surface. Si thickness reduction during the annealing was measured as shown in Fig. 1. The etching rate was ~0.01 nm/min at 1050 °C, and the etched thickness at zero minute in Fig. 1 was as high as 6.5 nm. Such an offset has not been so much discussed in the previous papers, but it indicates that Si is etched during the heating up and down steps in addition to the annealing at the target temperature. Especially during the heating up step, Si etching could be enhanced by inclusion of water or oxygen from the clean room air during the wafer loading. This offset value is too high to anneal thin SOI wafers, because the thickness reduction tends to degrade the thickness uniformity.

We introduced the vertical type heating apparatus exclusively designed for the hydrogen annealing. The wafers were loaded on a CVD-SiC coated boat at a few mm intervals, and were introduced into the process tube after purging the air in front of the tube to prevent from inclusion of water and oxygen. Hydrogen gas flew from the top to the bottom of the process tube after being purified by the heated palladium diffusion cells. Figure 2 shows time dependence of the etched thickness of Si in the temperature range from 1050-1200 °C. Note that the scales are as same as figure 1. The etching rate is apparently suppressed to 1/10 of 0.0013 nm/min at 1050 °C, and the offset is also reduced below 0.5 nm. That means, for example, SOI layer thickness is decreased below 1 nm at 1050 °C for 300 minutes in this new apparatus, while ~36.5 nm Si is removed in the epitaxial reactor.

In the vertical heating apparatus, the SOI surface was facing to the backside of another SOI wafers at intervals of a few mm. Figure 3 shows the influence of the facing surface material. At 1200 °C, the etching rate was 0.042 nm/min, when the SOI wafer was facing to Si, while the rate increased 9 times larger in case of the SOI wafer facing to SiO_2. This phenomenon suggests that SOI-Si could react with the facing SiO_2 in hydrogen ambient. Solid phase reaction between Si and SiO_2 are well-known, however, it has not been reported that Si and SiO_2 facing at a few mm interval react through hydrogen ambient. This was proved by Fig. 4, in which the numbers of removed Si atoms at Si surface calculated for the temperature range from 1100 to 1200 °C were coincide with that of SiO_2. In addition, such enhanced etching was not observed in the Ar atmosphere, but only in the hydrogen.

The temperature dependence of the etching rates were evaluated from the slopes of the time dependence of the etched thickness of Si and SiO_2 both in case of Si and SiO_2 chosen as the opposite surfaces (Fig. 5). As the activation energies derived from figure 5 indicate the similar values except the SiO_2-SiO_2 case, the same reaction could take place and control the etching of Si both facing to Si and to SiO_2. The following reaction is proposed to govern Si etching in this system.

$$Si + H_2 \rightarrow SiH_2 \uparrow$$

The reason why the Si etching is suppressed in Si-Si case is because SiH_2 is immediately saturated in the atmosphere between the wafers. In Si-SiO_2 case, SiH_2 generated at the Si surface is consumed at the SiO_2 surface as the following reaction, so that the Si etching reaction proceeds. SiO is known to have high evaporation pressure.

$$SiH_2 + SiO_2 \rightarrow 2SiO \uparrow + H_2O \uparrow$$

Finally, the etched thickness of ELTRAN wafers during hydrogen annealing are shown in figure 6. The etched thickness of the SOI layers were suppressed less than 1 nm by setting Si as the opposite surface, while SOI-Si was etched ~10 nm with relatively large deviation of 8 nm by facing to SiO_2.

4. Conclusion

We have applied hydrogen annealing for smoothing SOI surfaces. It was unveiled for the first time that the Si consumption was greatly suppressed thinner than 1 nm by annealing the SOI surface facing to Si in the specially designed vertical hydrogen annealing furnace. On the contrary, by annealing in the barrel type epitaxial reactor or facing SiO_2 in the vertical furnace, Si was consumed ten times larger than that of above. These phenomena are understood by investigating the reaction mechanisms. As a result, the uniform thickness with low surface micro roughness in ELTRAN is extended to extreme thin SOI as thin as 50 nm or less.

References

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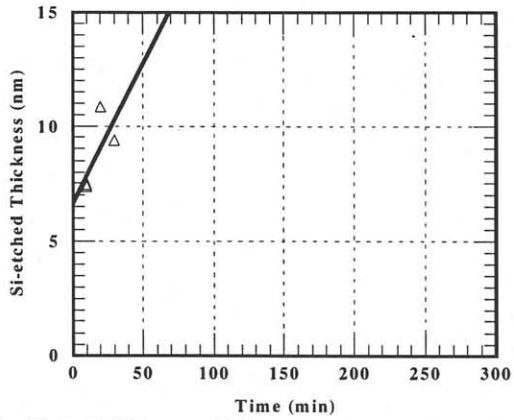

Fig. 1 Etched thickness of Si in a barrel type epi reactor. Annealing temperature is 1050 °C.

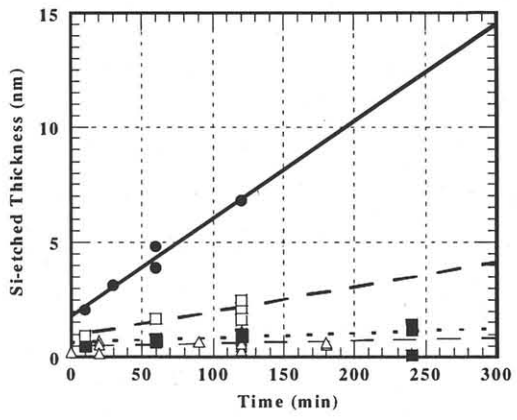

Fig. 2 Etched thickness of Si in a vertical heating apparatus. △ : at 1050 °C, ■ : at 1100 °C, □ : at 1150 °C, ● : at 1200 °C.

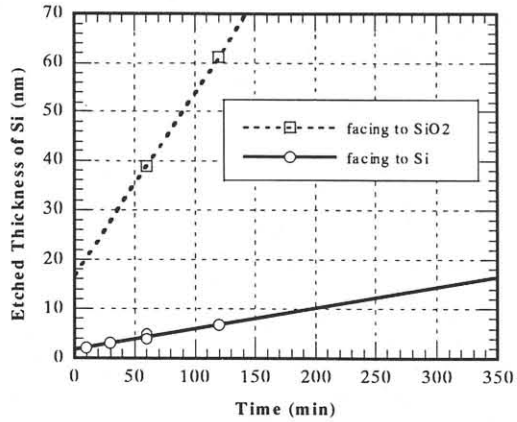

Fig.3 Etched thickness of Si during hydrogen annealing at 1200 °C. ○ : facing to Si, and □: facing to SiO_2.

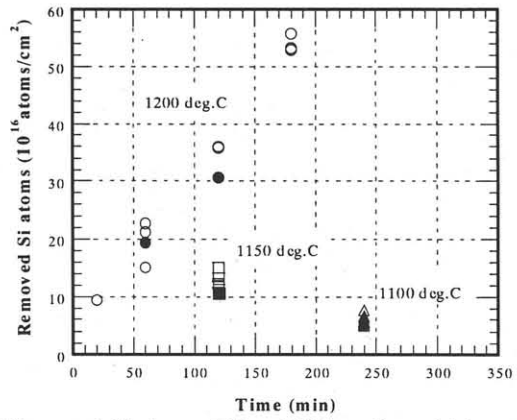

Fig. 4 Removed Si atoms at Si and SiO_2 surface which are faced each other. Open markers indicate SiO_2 surface, and closed markers are Si surface.

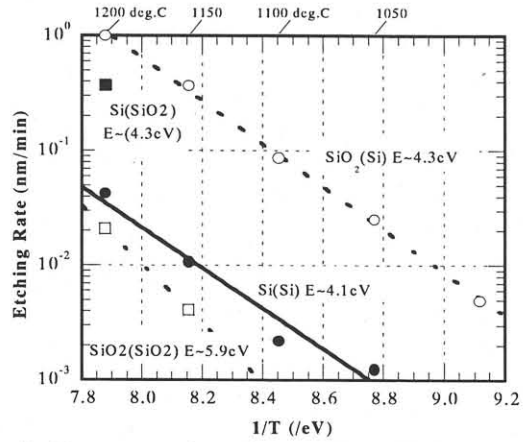

Fig. 5 Temperature dependence of the etching rate. ○: SiO_2 facing to Si, and □: facing to SiO_2, ●: Si facing to Si, and ■: facing to SiO_2.

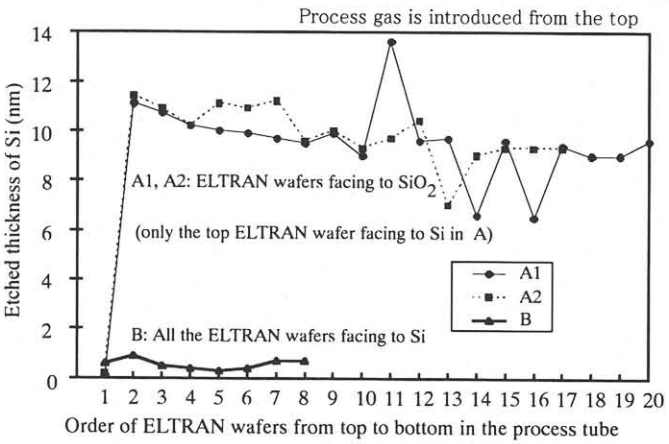

Fig.6 The opposite surface material dependence of the etched thickness of the ELTRAN wafers during hydrogen annealing at 1100 °C for 4hrs.