# Defect Engineering in Epitaxial Layers over Porous Silicon for ELTRAN<sup>®</sup> SOI Wafers

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### **1. Introduction**

In a silicon-on-insulator (SOI), an epitaxially grown Si layer is expected to be the SOI layer substitute for chochralski(CZ)-silicon, because the epitaxial layer gives the quite good gate oxide integrity (GOI) due to less crystal originated particles (COPs) which are currently reported as the killer defects for GOI on a CZ wafer.

We have already reported a SOI wafer using epitaxially grown Si by the epitaxial layer transfer (ELTRAN)<sup>1-4</sup> method. The epitaxial layer on porous Si was transferred onto a handle wafer to form a SOI wafer by bonding and etching back of porous Si with extremely high etching selectivity. In this paper, generation of stacking faults, which are the major defects, is investigated, and the density is significantly reduced to 50 /cm<sup>2</sup> by controlling both the porous structure and the heat treatment before the growth.

### 2. Experimental

The epitaxial layer was grown by the following treatments. A porous Si layer with 12  $\mu$ m-thick was formed by anodization of a (100) p<sup>+</sup> (0.01-0.02  $\Omega$ ·cm) CZ silicon wafer and was slightly oxidized including the pore-walls, as a preoxidation step, to prevent from beading up of the pores during the heat treatments such as epitaxy, oxidation and bonding annealing. Then, the wafer was dipped in diluted HF to remove thin oxide only at the surface region of the porous Si. The wafer was introduced into an epitaxial reactor to grow the epitaxial layer by CVD after prebaking in hydrogen atmosphere as a prebaking step. Two types of chambers were utilized for the epitaxial growth. One was a barrel type epitaxial reactor (Old), and the other was a single wafer processing reactor with a loadlock system (New). Stacking faults (SFs) in 2  $\mu$ m-thick epitaxial layers were measured by optical microscopy after Secco etching. The inspection areas were preferred to count SFs over 50-100. The delineated defects are the same in size, and XTEM revealed the origin of the SF was located at the surface of the porous Si.

#### 3. Results and Discussions

Figure 1 shows the prebaking temperature dependence of the stacking fault density. In the "old" reactor, the density was monotonously decreased by raising the temperature<sup>4</sup> from  $5.5 \times 10^5$  /cm<sup>2</sup> (1000°C) to  $1 \times 10^3$  /cm<sup>2</sup> (1150°C). Further reduction to  $3.5 \times 10^2$  /cm<sup>2</sup> was achieved by the preinjection technique, in which a small amount of Si source was introduced during the prebaking to help sealing surface pores. Unfortunately porous Si tended to deform at such high temperature prebaking and it sometimes resulted in difficulty of being etched off.

The "new" reactor gave an different result from the "old" one that the SF density had minimum value of  $2 \sim 3x10^2 / \text{cm}^2$ at relatively low temperature around 950°C, while it was as high as  $10^4 / \text{cm}^2$  in the higher temperature range over 1050°C. The high SF densities at a low-temperature end in both the reactors are presumably due to insufficient removal of the native oxide which would be formed by water or oxygen. On the contrary, the "new" reactor was designed to suppress the inclusion of water and oxygen into the reactors by the loadlock system and ultra clean gas supplying system so that the limiting temperature of the epitaxial growth was lowered.

Another question is why the SF density drops around 950

°C. We discovered that most pores at the porous surface were sealed by the hydrogen prebaking due to the surface diffusion of Si atoms<sup>3, 4</sup>. The surfaces of the porous Si before and after the prebaking in the "new" reactor were observed by scanning electron microscopy (SEM). The surface pores before the prebaking were ~10 nm in diameter and the density was around  $10^{11}$  /cm<sup>2</sup> as shown in Fig. 2. By prebaking at 1100 °C, the pore density was reduced in five order of magnitude to  $\sim 10^6$ /cm<sup>2</sup>, however, the residual pores were enlarged and mostly caved by coalescence of the adjacent pores as shown in Fig. 3. The surface-migrated Si atoms cannot seal all the pores due to the shortage of Si atoms. Note that the same scales are applied in Fig. 2, 3, and 5. Similar pore enlargement was also observed in case of the "old" reactor as shown in Fig. 4. In contrast, by prebaking at lower temperature of 950 °C, some pores were sealed, but the pore density was still  $10^{10}$ - $10^{11}$  /cm<sup>2</sup> as shown in Fig. 5. In addition, the enlargement of surface pores was mostly suppressed in comparison to the prebaking at 1100 °C (Fig. 3). These results suggest that stacking faults is introduced just above the relatively large residual pores among all the residual pores in the initial stage of the epitaxial growth. Stress localization around the residual pores would also play an important role. In the "new" reactor, less native oxide formation and its easy removal during the prebaking supports the minimization of the SF density around 950 °C.

The pore enlargement was suppressed by shortening the prebaking time. In addition, the small residual pores after this prebaking were effectively sealed by the preinjection, in which a small amount of Si was supplied at  $3 \times 10^{14}$  atoms/cm<sup>2</sup> sec. Under this condition, the surface diffusion of Si atoms was enhanced to seal the residual pores. As shown in Fig. 6, the SF density was lowered below  $2 \times 10^2$  /cm<sup>2</sup> by 2 second prebaking and the preinjection over 120 sec.

The porous structure also affects on the generation of the stacking faults in the epitaxial layer. It was found that the haze analysis by the laser light scattering particle analyzer such as Surfscan 6420 can monitor the structural difference of the porous Si. The haze is considered to reflect the porous structure near the surface including surface morphology, and was closely correlated to the SF density (Fig. 7). The current lowest SF density was 50 /cm<sup>2</sup> that was achieved by 2 second prebaking and preinjection at 950 °C for the porous Si with the haze of ~4.95 ppm. This epitaxial layer with low defect density was successfully transferred to ELTRAN SOI wafer, because the high etching selectivity was preserved due to low temperature epitaxy.

#### 4. Conclusion

In conclusion, the large residual pores were formed during sealing pores by the hydrogen high-temperature prebaking, and they were the generation sites of the stacking faults in the epitaxial layer. The SF density was reduced to  $50 / \text{cm}^2$ , so far, by controlling both the prebaking and the preinjection in a single wafer processing reactor with loadlock system. The haze level by a particle counter can monitor the porous structure, and well correlated to the SF density. Further reduction of the SF density is anticipated by controlling the preinjection steps and the porous structure.

## References

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- Fig. 1 Stacking fault density versus prebaking temperatures. □: in barrel type epitaxial reactor (prebaking for 450 sec),
  - $\triangle$ : in barrel type epitaxial reactor with preinjection (prebaking for 450sec), and
  - O: in single wafer processing reactor (prebaking for 120 sec).



Fig. 4 The oblique view of the residual pore observed by prebaking in the "old" reactor.



Fig. 6 Preinjection time dependence of the stacking fault density at 950 °C after prebaking for  $2 \sec(\bigcirc)$ , and  $120 \sec(\bigcirc)$ .

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Fig. 2 Surface morphology of the porous Si just before loading in the epitaxial reactor observed by SEM.



Fig. 3 The residual pores observed after 1100 °C prebaking for 2 sec. (a) enlarged pore, and (b) coalesced pore.



Fig. 5 Surface morphology of the porous Si after 950 °C prebaking for 2 sec.



Fig. 7 Correlation between the stacking fault density and the haze of porous Si. Epitaxial growth after prebaking (120 sec) at 1100 °C( $\Box$ ), prebaking (120 sec) at 950 °C( $\triangle$ ), and prebaking (2 sec) at 950 °C( $\bigcirc$ ).