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Analysies of the Radiation Caused Characteristics Change in SOI MOSFETS Using Field Shield Isolation

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1. Introduction

Equipment in nuclear power plant and satellites in cosmic space are exposed to irradiated environment. Thus the reliability of radiation in LSI becomes an important issue[1].

SOI MOSFETs are attractive devices due to soft errors free in addition to high speed and low power performance. However it is reported that leakage current by radiation occur in SOI MOSFETs with LOCOS isolation[1]. Fig.1 shows schematic diagram of radiation ionizing effect. Electron-hole pairs are generated by radiation in the oxide. Holes are trapped at interface of buried oxide and LOCOS oxide, because hole's mobility is small as compared with electron. Trapped holes induce parasitic MOSFET. Therefore, sufficient radiation-tolerant technology of isolation is needed in an radiation environment[1].

In this paper, it is described that we analyzed radiation effects on device characteristics in SOI MOSFETs. Moreover characteristics changes in subquater micron MOSFETs are also analyzed for device design.

2. Fabrication Process

Fig.2 shows an SOI MOSFET electrically isolated by FS isolation. Cobalt salicide was used to lower resistivity. SIMOX wafers were applied with a buried oxide(BOX) thickness of 370nm.

Irradiation tests were performed for FS-isolated 0.35μm SOI MOSFET at a level of 10^5rad (Si) from a Co^{60} source at room temperature. During radiation testing, bias conditions for nMOS were Vg=2.0V, Vd=Vs=Vbody=0.0V, and for pMOS, Vg=0V, Vd=Vs=Vbody=2.0V, which estimates actual operation conditions.

3. Results and discussion

Fig.3 shows Id-Vg characteristics for LOCOS-isolated SOI MOSFETs. Leakage currents in the LOCOS edge were not observed for pMOS. However, leakage current was observed after radiation in nMOS as previously reported [2],[3]. This is because trapped holes generated by radiation induce a leakage current at the LOCOS edge.

Fig.4 shows Id-Vg characteristics for FS-isolated SOI MOSFETs before and after radiation exposure. Radiation conditions were the same as those of LOCOS sample. A clear difference is revealed in the case of nMOS. In contrast to the LOCOS data, there is no radiation-induced leakage current in FS isolation. Subthreshold swing and threshold voltage is preserved even after radiation exposure.

For the sake of estimating trapped hole density at the SOI/BOX interface, back channel current as a function of substrate bias was measured. Fig.5 shows the threshold voltage difference before and after radiation exposure. The threshold voltage difference is 19V, which means the trapped hole density can be estimated as $1.06\mathrm{x}10^{12}\mathrm{cm}^{-2}$. This value is reasonable with another report [4].

Fig.6 shows simulation results of the potential contours at the LOCOS edge when trapped holes with density of $1.0\mathrm{x}10^{12}\mathrm{cm}^{-2}$ were set at SOI/BOX interface. The LOCOS edge was doped with high boron concentration against punch through. The potential rise was seen at the edge portion. Leakage current flows in this LOCOS edge[4]. Fig.7 shows simulation results of the potential contours in FS-isolated SOI MOSFET when trapped holes $1.0\mathrm{x}10^{12}\mathrm{cm}^{-2}$ were set at the SOI/BOX interface. The SOI thickness is 100nm and the gate voltage is 0.56V. A potential rise is not seen in FS edge.

Fig.8 shows Id-Vg characteristics for edgeless SOI MOSFETs. The transistor characteristics are almost the same as that of FS-isolated MOSFETs. This indicates that isolation-related issues for radiation do not occur in the FS-isolated MOSFETs.

Fig.9 shows simulated dependence of threshold voltage shift on channel length in an SOI nMOSFET. Short channel effects with trapped holes become intense at channel length of 0.18μm. Fig.10 shows simulated result of potential in SOI nMOSFET with channel length of 0.18μm near SOI/BOX interface. The back channel potential increase due to trapped holes occur at the BOX/SOI interface, hence degrading the short channel behavior. Short channel effects in radiation environment are severer than those in a non-radiation one, so that we must consider this when designing deep submicron devices used in irradiated environment.

4. Conclusion

We analyzed the effect of radiation on isolation of SOI MOSFETs.Leakage current which was observed in LOCOS isolated SOI MOSFETs has been successfully suppressed by field shield isolation.

References

[1]IEEE Spectrum, March , p36, 1998.
[2]C.Brisset, et al., IEEE Nucl.Sci., 43, p2561,1996.
[3]T.Iwamatsu, et al. J.J.A.P , 36, p1631, 1997.
[4]S.T.Liu, et al. IEEE Nucl.Sci., 44, p2101,1997.

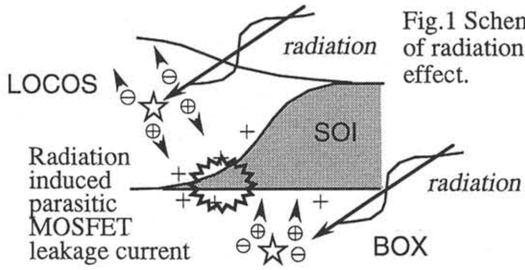

Fig.1 Schematic diagram of radiation ionizing effect.

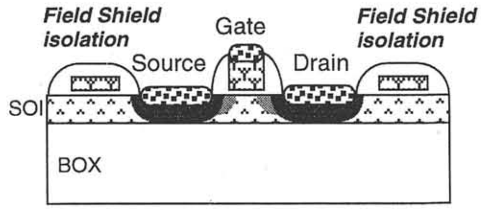

Fig.2 Field shield isolated SOI MOSFET

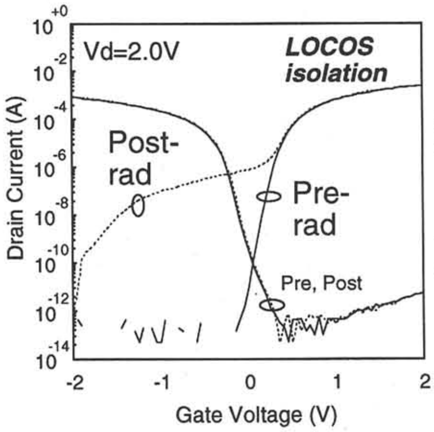

Fig.3 Id-Vg characteristics for pre- and post-radiation in LOCOS isolated SOI MOSFETs.

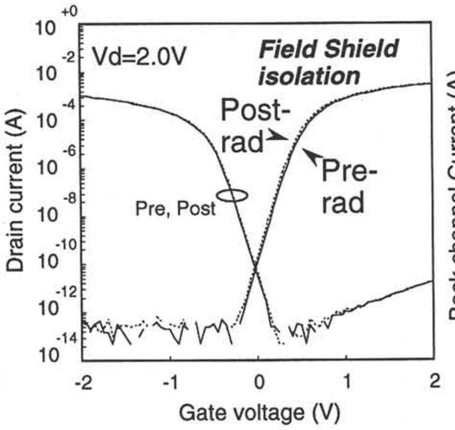

Fig.4 Id-Vg characteristics for pre- and post-radiation in FS-isolated SOI MOSFETs.

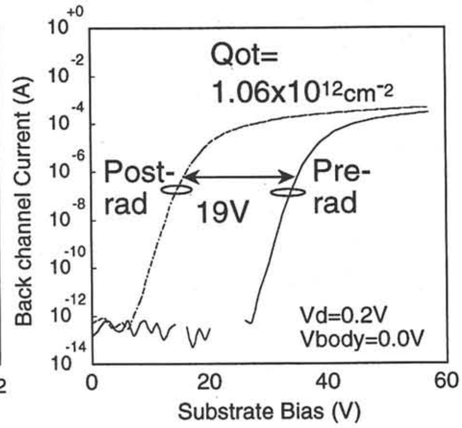

Fig.5 Back channel characteristics for pre- and post- radiation in edgeless-SOI nMOSFET. L=0.6um.

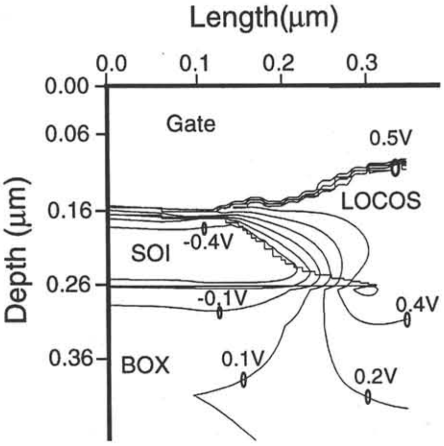

Fig.6 Simulated potential contours of LOCOS-isolated SOI nMOSFET. Hole trap density of $1x10^{12}cm^{-2}$ was at SOI/BOX interface.

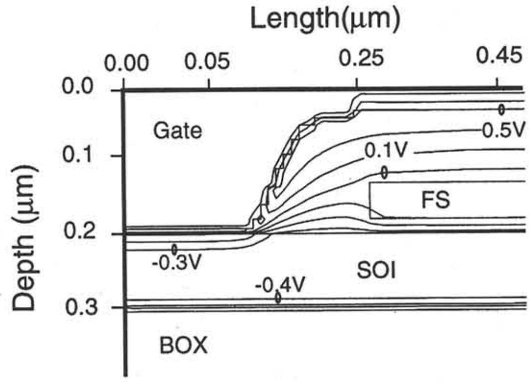

Fig.7 Simulated potential contours of FS-isolated SOI nMOSFET. Hole trap density of $1x10^{12}cm^{-2}$ was at SOI/BOX interface.

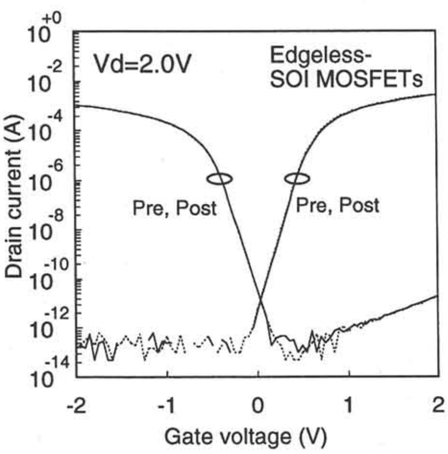

Fig.8 Id-Vg characteristics for pre- and post-radiation in edgeless- SOI MOSFETs.

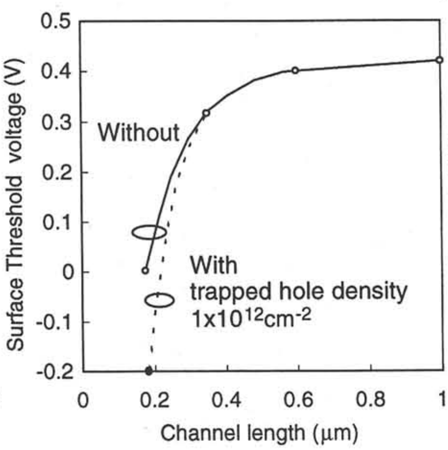

Fig.9 Simulated dependence of threshold voltage shift on channel length in a SOI nMOSFET including trapped charge effects.

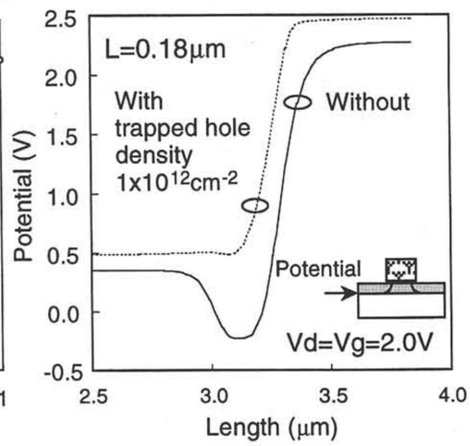

Fig.10 Simulated potential in a SOI nMOSFET with channel length of 0.18μm.