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Distortion Analysis of SOI MOSFETs for Analog Applications

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1. Introduction

While high performance low voltage SOI digital circuits have been achieved [1], further study of device-based analog issues is required to realize the implementation of SOI CMOS in mixed-mode applications. Previous studies [2, 3] have demonstrated the potential improvements offered by SOI technology in OpAmp and other analog circuits. However, a few critical issues, such as distortion in SOI devices and the impact of floating body effects have yet to be studied in detail. In this work, small signal and large signal harmonic distortion in SOI single transistor amplifiers were studied. The floating body induced degradation of harmonic distortion was also addressed.

2. Devices and Measurements

In order to evaluate the impact of floating body effects on distortion in different SOI MOSFETs, a common source single transistor amplifier was built. Motorola thin film SOI nMOSFETs, with two types of layout, were used in this study: (i) floating body SOI nMOSFETs, including both partially-depleted (PD) and fully-depleted (FD) devices achieved by adjusting the threshold implant, and (ii) H-gate PD body-tied devices [7]. Harmonic distortion was measured using an HP 3561A dynamic analyzer, an HP 3324A function generator (operated at 1 kHz to avoid the input capacitance effect), and a bias network with a load resistance $R_D > 10 \times r_0$.

3. Small Signal Analysis

In a nonlinear system, a pure sinusoidal input signal results in an output signal which includes the sinusoidal signal as well as higher harmonics. The corresponding i-th order harmonic distortion can be expressed as follows [4],

$$HD_i \propto \frac{\partial^i}{\partial V_{gs}^i} V_{ds} = \frac{\partial^{i-1}}{\partial V_{gs}^{i-1}} (g_m / G_{DS}) = \left(r_0 \cdot \frac{\partial^{i-1}}{\partial V_{gs}^{i-1}} g_m\right) + (r_0 \text{ distortion}). \quad (1)$$

In long channel MOSFETs, since $G_{DS}(= 1/r_0)$ is almost bias

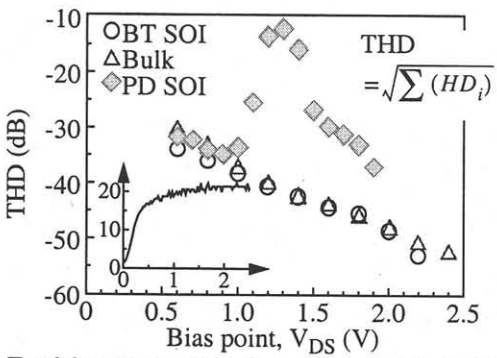

Fig. 1 Total harmonic distortion of a good body-tied (BT) SOI, bulk, and PD floating body SOI nMOS as a function of V_{DS} with 0.4 V output swing. The inset shows the V_{DS} dependence of r_0 of a BT SOI nMOS at $V_{GT} = 0.1$ V.

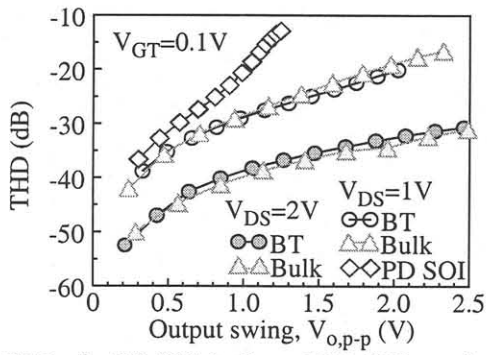

Fig. 2 THD of a BT SOI, bulk, and PD SOI as a function of peak-to-peak output swing as devices biased at low voltage (1V) and high voltage (2V) operations.

independent, the harmonic distortion is dominated by g_m distortion, which has been well-examined [5]. However, in both submicron bulk and good body-tied SOI nMOSFETs, output resistance r_0 (= $1/G_{DS}$) can not simply be modeled by a constant early voltage [6]. In order to demonstrate the effect of this non-linearity of r_0 on harmonic distortion, we can adopt an inverse harmonic distortion analysis, expressed as:

$$HD_{2,inv} \propto \frac{\partial^2 V_{gs}}{\partial V_{ds}^2} = \frac{\partial^2}{\partial V_{ds}^2}\left(\frac{G_{DS}}{g_m}\right) = \left(\frac{1}{g_m} \cdot \frac{\partial G_{DS}}{\partial V_{ds}}\right) + (g_m \text{ distortion}). \quad (2)$$

This equation has been shown to be equivalent to that for HD_2 by Bult [4]. The V_{DS} dependence of r_0 (inset of Fig. 1) increases the distortion at the low drain biases (Fig. 1), which is a major concern for low-voltage applications.

4. Floating body induced r_0 distortion

Previous work [8] has shown that a good body-tied SOI device can provide similar linearity to bulk devices for either low or high voltage applications with large output swing, as shown in Fig. 2. On the other hand, in PD floating body SOI nMOSFETs, as V_{DS} increases, the charging of body causes an output kink (due to V_{TH} reduction) and induces a spike in G_{DS} [7]. It can be seen that the THD may be strongly degraded when the device is biased close to the onset of the kink (peak of $\partial G_{DS}/\partial V_{ds}$). Figure 2 shows the THD of a PD floating body SOI nMOS as a function of drain bias. Below kink onset voltage at 1 kHz (~ 1.1 V), its distortion is similar to those of bulk and good body-tied SOI nMOSFETs. Approaching the kink, the THD is drastically degraded as expected.

It is also necessary to understand the large signal distortion behavior which can not be predicted by small signal analysis. When biased in the pre-kink region (V_{DS} = 0.75 V), PD SOI amplifiers exhibit a similar linearity to that of good body-tied devices (Fig. 3) for small output swings. However, as the output swing reaches the kink, third-order harmonic distortion (HD_3) drastically increases which precludes the

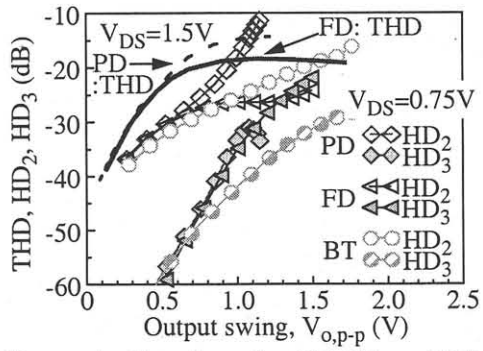

Fig. 3 Harmonic distortion of a BT, FD, and PD floating body SOI nMOS as a function of output swing at V_{GT} = 0.1 V. The devices were biased in pre-kink (0.75 V) and post-kink (1.5 V) regions.

use of PD SOI in wide dynamic range applications. Shifting from PD to FD, floating body effects are suppressed due to the reduction of the source/body junction barrier, which results in a weaker output kink [8]. As a result, the FD SOI amplifiers achieve second-order harmonic distortion (HD_2) levels compatible with those of BT SOI. However, FD SOI provides only limited improvement compared to PD SOI in terms of HD_3. On the other hand, when biased in the post-kink (1.5 V) region, the SOI amplifier performance degrades due to both the reduced transistor intrinsic gain (due to the increase of G_{DS}) and the large increase in harmonic distortion for both PD and FD floating body SOI nMOS (Fig. 3). Therefore, in baseband analog circuits, distortion issues such as the sensitivity of HD_3 to the kink restrict the use of floating body devices in large dynamic range applications. Good body-tied SOI devices, which provide compatible linearity with bulk devices, can be an alternative solution.

5. Non-ideal body-tied effects

Figure 1 has shown that a good body-tied SOI nMOS can eliminate unwanted floating body effect to offer low distortion performance. However, the finite neutral body underneath the gate results in a high resistance body discharging path. This leads to a local floating body effect resulting from the non-uniform body voltage distribution across the body of an H-gate body grounded SOI nMOS [11]. Figure 4 shows the G_{DS} of a non-ideal body-tied (N-BT) and a good body-tied SOI nMOS. Their G_{DS} curves start to diverge as the drain bias increases beyond 1.5 V. Three operating regions were characterized, as shown in Fig. 5. At low voltage (0.75 V), N-BT SOI and BT SOI nMOS achieve similar HD_2 and HD_3 performance. However, at the point where their G_{DS} curves diverge (1.5 V) due to the local floating body effect, the non-ideal body-tied device experiences a drastic degradation in HD_3 due to the sharp peak in $\partial^2 G_{DS}/\partial^2 V_{ds}$ caused by a large increase in $\partial G_{DS}/\partial V_{ds}$. At high voltage (2 V), HD_2 degrades due to both the increases of G_{DS} and the non-zero $\partial G_{DS}/\partial V_{ds}$. But, HD_3 decreases due to the diminishing $\partial^2 G_{DS}/\partial^2 V_{ds}$.

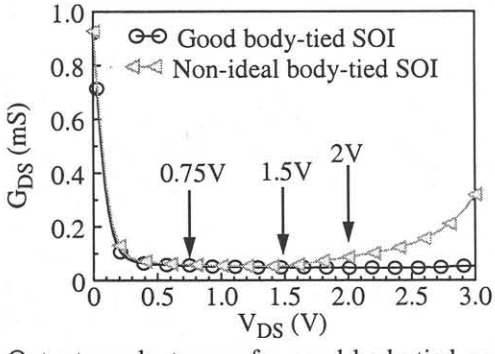

Fig. 4 Output conductance of a good body-tied and a non-ideal body-tied SOI nMOS at V_{GT} = 0.1 V. The arrows indicate the three operation regions.

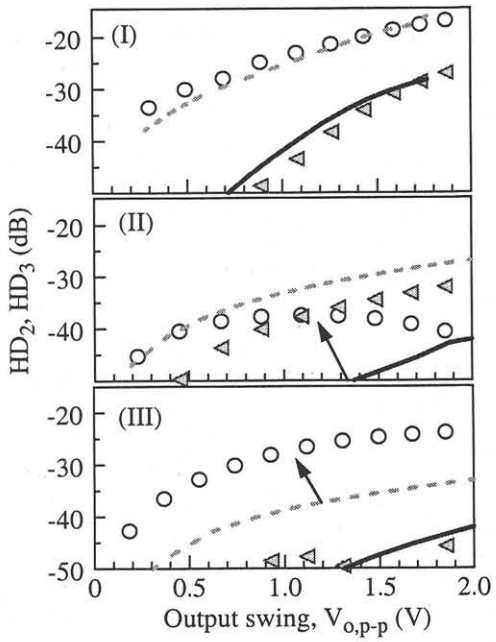

Fig. 5 Harmonic distortion of a non-ideal body-tied (N-BT) and a good body-tied (BT) SOI nMOS as a function of output swing at V_{GT} = 0.1 V. (I): V_{DS} = 0.75 V. (II): V_{DS} = 1.5 V. (III): V_{DS} = 2 V. (○: HD_2 of N-BT, ◁: HD_3 of N-BT, dash line: HD_2 of BT, and solid line: HD_3 of BT). The arrows indicate the increase of HD_i in N-BT.

6. Conclusion

The distortion observed in different SOI MOSFET technologies has been analyzed in detail and the relevant circuit issues were identified. For low voltage operation, floating body SOI devices can be used in small output swing applications. However, a kink in floating body device and non-ideal body-tied effects in body grounding device can degrade linearity, specially for third order harmonic distortion. As a result, for normal voltages (e.g. 3 V) or large dynamic range cases, it is necessary to use body-tied SOI devices optimized for low distortion.

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