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# The OFF-State Leakage Current in Ultra-Thin SOI MOSFET's

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## 1. Introduction

The controllability of the Short-Channel Effects (SCE) and the OFF-state current of low-Vth (<0.3V) MOS transistors becomes a major challenge for low-voltage, low-power dissipation LSI's. In this context, SOI is recognized to offer several advantages for low-voltage operation [1-2]. Fig.1 compares the OFF current dependence on threshold voltage for 0.35μm gate length BulkSi, and Fully Depleted (FD) n-MOSFETs fabricated on 50 nm superficial top Si film on SIMOX wafers [2]. The advantages of SOI are clear. The impact ionization and floating body effects, however, enhance *Vth* lowering as the drain voltage increases [3] and contribute to increase the OFF-state current as illustrated in Fig.2 for SOI n-MOSFETs with different *Vth*'s. To explain the experimental results and assess the transistor design it is essential to have a quantitative and physical model of the leakage current.

In this paper, the OFF-state leakage current in ultra-thin SOI MOSFET's is analyzed including (i) impact ionization, (ii) parasitic bipolar action, and (iii) floating body effects. A model is presented that gives physical insight on the device parameters determining the leakage current at low voltage.

## 2. OFF-state Current in SOI

The OFF current in a MOS transistor is defined as the drain current at $Vgs$=0V, $Idoff = Id(Vgs=0V)$. As the drain voltage $Vd$ increases, majority carriers generated by impact ionization accumulate at the minimum of potential and form a quasineutral body region that acts as the base of the parasitic bipolar transistor. Fig.3 illustrates the SOI MOSFET and its equivalent circuit including the parasitic bipolar transistor and the impact ionization current $Ii=(M-1)/[1-\beta(M-1)]\cdot Ich$. With $Ich$ the channel current and $\beta$ the bipolar current gain. $M$ is the impact ionization multiplication coefficient, $(M\text{-}1)=Ai\ Vd\ \exp(-Bi\ \lambda/Vd)$, with $Ai$ and $Bi$, the impact ionization constants and $\lambda$ is the SCE characteristic length [3]. The bipolar action is modeled using the Ebers-Moll equations [4]. For subthreshold operation $Ich = Io\ \exp(q(Vgs\text{-}Vth)/kT)$. The threshold voltage $Vth$ is then affected by the back-gate effect, $Vth = Vtho - \sigma Vd - \gamma Vbs$. Where $\sigma$ is the low-Vd Drain Induced Barrier Lowering (DIBL) parameter, and $\gamma$ is the linearized back-gate effect coefficient. For a FD device and using Fig.3 equivalent circuit, $\gamma \fallingdotseq Csi/Ctox$. The OFF-state current is expressed as

$$Idoff = \left(\frac{M}{1-\beta\cdot(M-1)}\right)\cdot Io\cdot\exp\left(-\frac{Vtho-\sigma\cdot Vd-\gamma\cdot Vbs}{m\cdot kT/q}\right) \quad (1)$$

and the source-body potential is obtained by solving the circuit equations in Fig.3.

$$Vbs \cong \frac{n\cdot kT/q}{\left(1-\gamma\frac{n}{m}\right)}\cdot\ln\left((\beta+1)\cdot\left(\frac{Icho}{Ijo}\right)\cdot H(Vd,\beta)+1\right) \quad (2)$$

$$H(Vd,\beta)=\frac{(M-1)}{1-\beta\cdot(M-1)},\quad Icho = Io\cdot\exp\left(-\frac{Vtho-\sigma\cdot Vd}{m\cdot kT/q}\right)$$

$n$ and $Ijo$ are the ideality factor and the reverse current of the source-body diode, respectively. The SCE is included in $Vtho$ and $\beta$.

## 3. Comparison with Experimental Devices

Salicided Fully-Depleted SOI n-MOSFET's fabricated on SIMOX wafers with 50nm thick top Si, 100nm buried oxide and 7nm gate oxide are considered in this study [2].

From the data in Fig.1, $Io$ is estimated to be $2\times10^{-7}$A/μm. Fig.4 compares the measured and calculated OFF current for the n-MOSFETs of different gate lengths. The agreement with the model proposed here is excellent. $Ijo$ was the only fitting parameter ( $Ijo$~$10^{-14}$A/μm). The breakdown voltage occurs when $\beta\cdot(M\text{-}1)\rightarrow1$. The exponential dependence of $Idoff$ on $Vd$ on short-channel devices corresponds to the regime where the floating body and back-gate bias effects dominate the leakage . According with the derived model, even when $\beta\rightarrow0$, impact ionization and floating body effects are enough to rise $Vbs$ and increase $Idoff$. Fig.5 illustrates the effect of $Vth$ on $Idoff$. Again, good agreement with the model is obtained. From eq.(2), the on-set for the floating body dominated leakage is determined by the source-body diode characteristic ($n$, $Ijo$), the ($Icho/Ijo$) ratio and the impact ionization critical voltage ($Bi\cdot\lambda$) [3]. $Ijo$ can be increased by the introduction of band gap engineering [5] or Ar implantation to reduce lifetime [6]. The effect of the critical voltage ($Bi\cdot\lambda$) indicates a tradeoff between a wide supply voltage margin (large $\lambda$) and SCE controllability (small $\lambda$).

The proposed analysis and model describe the effect of all important parameters on OFF-state current. The rapid increase of IOFF at low-$Vd$ for ($Vbs > (Vtho - \sigma Vd)/\gamma$), imposes a limit on the maximum supply voltage (~ 1.3V for the devices in Fig.2) for low leakage stable operation. The physical insight given by this new model proved useful in transistor design and technology optimization.

## References

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[5] M.Yoshimi et al., IEEE Intern.SOI Conf., pp.80-81, Oct.1995.
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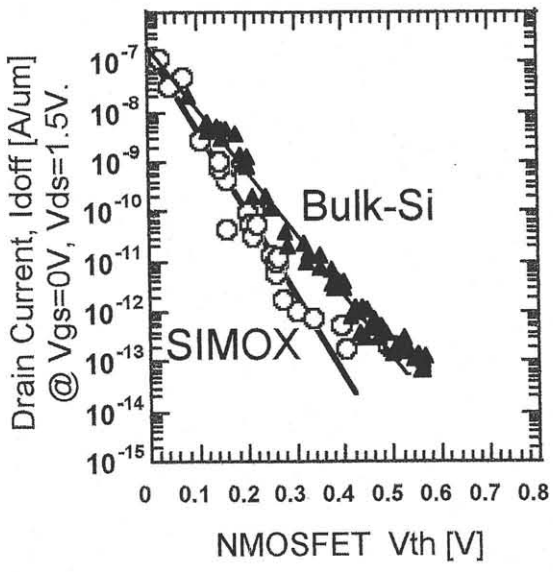


Fig.1: Comparison of OFF-state NMOSFET current for 0.35μm gate length BulkSi and Fully-Depleted SOI devices.

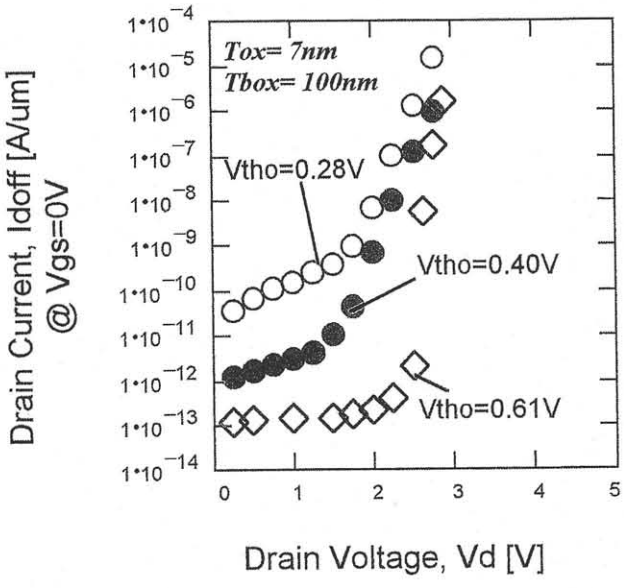


Fig.2: OFF-sate leakage current Vs drain voltage for 0.35μm FD n-MOSFETs fabricated on 50nm top Si film on SIMOX wafers [2]. Low Vth and floating body effect increase OFF current at low drain voltage.

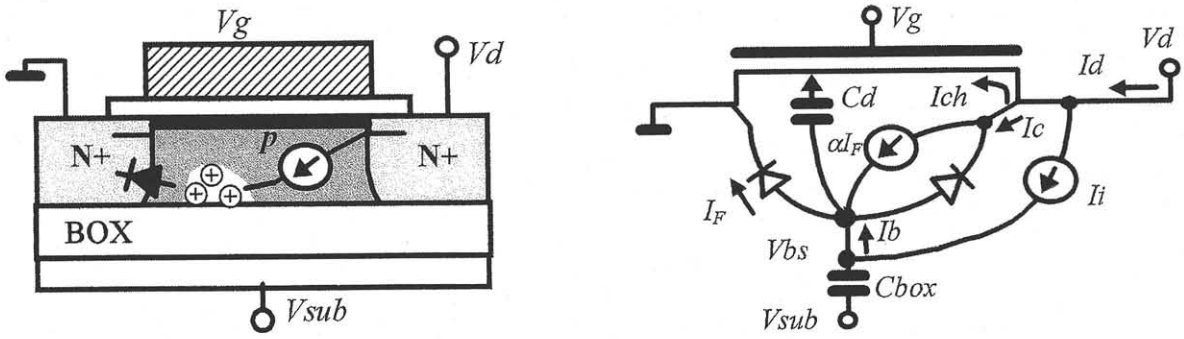


Fig.3: SOI MOSFET equivalent circuit for static operation including the impact ionization *Ii* and the parasitic bipolar transistor.

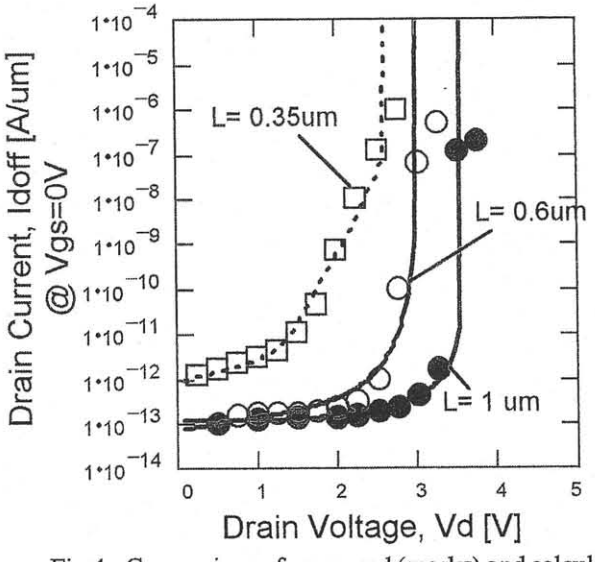


Fig.4: Comparison of measured (marks) and calculated (lines) SOI NMOSFET's OFF current Vs drain voltage for different gate lengths.

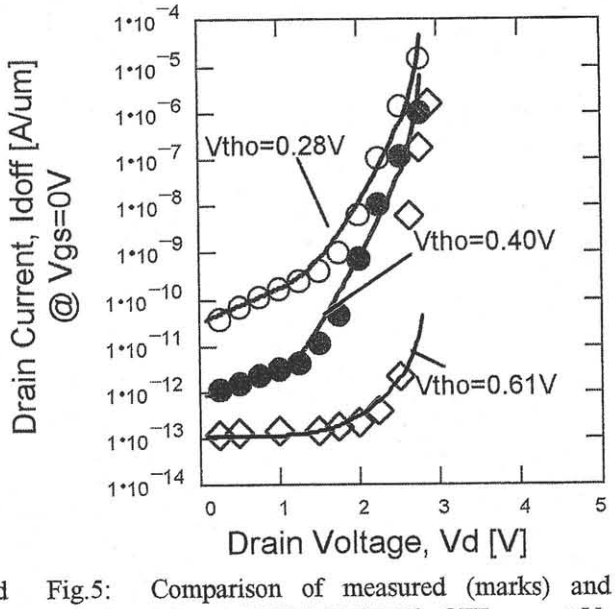


Fig.5: Comparison of measured (marks) and calculated (lines) SOI NMOSFET's OFF current Vs drain voltage for different Vth's, and L=0.35μm.