Fabrication of 40-150nm Gate Length Ultrathin n-MOSFETs Using ELTRAN SOI Wafers

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1. Introduction
The main issue in microelectronics is how far SiMOSFETs can be scaled in future VLSI's [1],[2]. It is essential to avoid the short channel and punch-through effect even in such short channel devices. It has been pointed out that a thin active Si layer with a backside conducting layer [1],[3] and an ultra-shallow source and drain junction [4],[5] are effective. However, the systematic experimental works on ultra-short channel MOSFETs have been insufficient. In this paper, we report the fabrication of ultra-thin SOI n-MOSFETs in the 40-150nm gate length regime, and demonstrate the excellent threshold voltage roll-off characteristics.

2. Device Fabrication
The ultra-thin SOI n-MOSFETs shown in Fig.1 were fabricated on SOI wafers prepared by the epitaxial layer transfer (ELTRAN) technique. The major process steps are shown in Fig.2. A LOCOS process was used for both device isolation and SOI thinning for channel regions (10-20nm in thickness). EB lithography was adopted for device region (0.6-1.2μm in length) and gate poly-Si patterning (40-150nm in length). The gate poly-Si (n) was shaped by ECR plasma etching. We did not find any damage in the thin gate oxide (4.7nm in thickness) after the EB lithography and ECR etching as depicted in the C-V curve in Fig.3. It is apparent from the SIMS data in Fig.4 that ultra-shallow source/drain P diffusion (~10nm in depth) was achieved by RTA at 870°C for 10sec from a spin-coated PSG film.

3. Result and Discussions
The electrical characteristics were measured at the backside voltage of 0V at room temperature. The fabricated 40-150nm gate length SOI n-MOSFETs operate quite normally as typically shown in Fig.5. The effective channel length of each device is deduced to be around 20nm less than the gate length, considering the SIMS analysis in Fig.4. The threshold voltage and S-factor are shown in Fig.6 as a function of the gate length with the SOI thickness as a parameter. It should be noted that the ΔVth for the 40nm gate length device with tsox=11nm is only around 0.2V with respect to that for the long channel one (Lg=150nm). The S-D series resistance was 1-1.5kΩ. If the S-D series resistance would be reduced, the g_m would be expected to be improved significantly. Figure 6 says that further improvement in the roll-off characteristic is expected by reducing the SOI thickness.

4. Conclusions
In summary, ultra-short gate length, and ultra-thin SOI n-MOSFETs have successfully been fabricated. The 40-150nm gate length devices show the excellent roll-off characteristics. The effectiveness of an ultra-thin SOI layer to prevent the short channel effect was experimentally confirmed.

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References
Fig. 1 Schematic cross section and the SEM photograph of the 40nm gate length ultra-thin SOI n-MOSFET. The gate width is 5μm.

Fig. 2 Fabrication processes for 40-150nm gate length ultra-thin SOI MOSFETs.

Fig. 3 Experimental C-V curve after the EB lithography and ECR gate poly-Si etching.

Fig. 4 SIMS profiles of solid-phase diffused phosphorus from the spin-coated PSG film by RTA: (a) 870°C, 10min, (b) 900°C, 10min.

Fig. 5 \( I_d-V_d \) (5(a)) and \( I_d-g_{m}-V_g \) (5(b)) characteristics of the 40nm gate length ultra-thin SOI n-MOSFET.

Fig. 6 Threshold voltage and S-factor vs. gate length characteristics for the different channel layer thickness (t_{SOI}=11nm, t_{SOI}=18nm) SOI n-MOSFETS.