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Performance and Reliability Improvement of Polycrystalline Silicon Thin Film Transistors by Deuterium Plasma Passivation

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1. Introduction

Reliability of poly-Si TFT's has become an important issue for devices after long term operation. Several studies [1-2] have shown that the degradation of poly-Si TFT's was mainly resulted from the conduction of a large amount of carriers, which cause the creation of metastable states. A widely used method to improve device performance and reliability of poly-Si TFT's is by way of hydrogenation. In this paper, the device performance and reliability of a LTP (Low-Temperature Processed) poly-Si TFT with deuterium plasma passivation will be studied. It was found that replacing the hydrogen (H_2) with the deuterium (D_2) will improve enormously the TFT performance, in particular the mobility and reliability. The advantages of the deuterium process is attributed to the giant isotope effect and strong coupling efficiencies by the Si-D bonds.

2. Device Fabrication

Low temperature poly-Si TFT's are made with a maximum processing temperature of 600°C. Undoped 100nm-thick amorphous silicon films were re-crystallized, which contain grains with an average size of 0.1-0.2 μm. After island definition, a 34nm-thick liquid phase deposited (LPD) gate oxide and a 350nm-thick polysilicon gate electrode films were deposited and patterned. Source/drain and gate electrodes were doped by self-aligned phosphorus implantation. The remaining fabrication procedures are similar to earlier reports [3]. Hydrogen and deuterium plasma passivation were performed respectively until 3hr at 300°C before the growth of the TEOS-oxide interlayer. The devices are conventional top-gate structures as shown in Fig.1.

3. Results and Discussion

Fig. 2 shows the measured transfer characteristics for LTP poly-Si TFT's with hydrogen and deuterium plasma passivation, respectively. The control sample is also shown for comparison. It is clear that the D_2 sample or the H_2 sample improves largely the ON-state and OFF-state characteristics. Table 1 is the calculated device parameters of the above three samples. The field effect mobility (μ_{eff}), can be improved much better in the D_2 sample. Fig. 3 shows the energy distribution of the density of states (D_{it}) before and after the stress for both D_2 and H_2 samples [4]. From the pre-stress data, the D_2 sample has the smaller band-tail trap states than that of the H_2 sample, implying that the D_2 sample has better passivation efficiency with the strained-bonds and then effectively reduces its band-tail trap states.

For the hot carrier stress measurement, a dc stress at $V_{DS}=V_{GS}=$ 20V for both D_2 and H_2 samples were performed until 10^4sec. Fig. 4 shows the comparison of reverse-mode output characteristics for both D_2 and H_2 samples before and after 200 sec stress. Fig. 5 shows the ON current degradation with stress time for both D_2 and H_2 samples. The degradation of the D_2 sample is much smaller than that of the H_2 sample at the beginning of stress. As the stress time continues, the degradation of both two samples approaches with each other. Two-degradation mechanisms have been found, one is the *trap-state-induced* degradation and the other one is *hot-carrier-induced* degradation. At the beginning of the stress time duration, the hot carrier degradation was dominant by inspecting the reverse-mode output characteristics. When the stress time continues, the trap-state-induced degradation was important, which can be confirmed by inspection of the gradually non-local degradation of output characteristics. As shown in Fig. 4, the D_2 sample has much better immunity to the hot carrier degradation. It can be further found in Fig. 5 that the D_2 sample has two slopes in current degradation rather than that of the H_2 sample. It is believed that the two slopes could be resulted from the two degradation mechanisms. Fig. 6 shows the threshold voltage shift (ΔV_T) and trap state density (ΔN_t) variations on the stress time for both D_2 and H_2 samples, in which D_2 sample has smaller degradation than that of the H_2 sample. In addition, the two device parameters (V_T,N_t) have a similar degradation trend, which implies that the generated N_t is responsible for the increase of V_T. The V_T shift is usually related to the variation of deep states. As shown in Fig. 3, the deep states are obviously increased after a long-term stress compared with the band-tail states, and hence, leads to a large V_T shift, which is therefore consistent with the result in Fig. 6. Fig. 7 shows the comparison of transfer characteristics for poly-Si TFT's with the D_2 and H_2 plasma passivation before and after the stress. It is obvious that the D_2 sample is still better in reliability than the H_2 sample. Since the deep states are generated after stress for both samples, the degradation of subthreshold swing (S) is reasonable. Fig. 8 shows the measured $\Delta\mu_{eff}$ and ΔS on the stress time for both D_2 and H_2 samples. Degradation of both parameters in the D_2 sample is also smaller than that in the H_2 sample. Moreover, the variation of μ_{eff} is smaller than the swing(S) after the stress, which implies again that the generated defects are the deep states rather than the tail states. From the above results, the deuterium plasma passivation obviously improves the reliability of poly-Si TFT's. Therefore, we conclude that the advantages of the deuterium passivation can be understood to be the giant isotope effect and stronger coupling efficiency between the Si-D wagging mode and the Si-Si lattice mode.

5. Conclusions

In conclusion, it was demonstrated that the poly-Si TFT's passivated in either deuterium or hydrogen plasma can both improve the device performance and reliability. In particular, the deuterium-passivated TFT's improve the field effective mobility much better than the hydrogen-passivated TFT's as a result of a more effective passsivation in the band-tail trap states. We proposed two types of degradation mechanisms, trap-state-induced degradation and the hot-carrier-induced degradation to explain the D_2 passivation effect. In terms of the reliability improvement, replacing the hydrogen with the deuterium plasma reduces greatly the device degradation for both mechanisms. The reasons for a better performance of the deuterium plasma passivation on the device degradation can be understood to be the giant isotope effect and strongly coupled efficiency between the Si-D wagging mode and the Si-Si lattice mode.

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References

1) M. Hack et al.:*IEEE Trans. Electron Devices*, (1993), p. 890.
2) I. Wu et al.: *I IEEE Electron Device Lett.*, (1990), p. 167.
3) C. Yang et al.: *I EEE Electron Device Lett.*, (1994), p. 389.
4) G. Fortunato.: Appl. Phys. Lett., (1986), p. 1025.

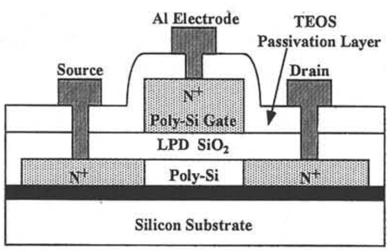

Fig. 1 Cross-sectional view of a LTP poly-Si TFT.

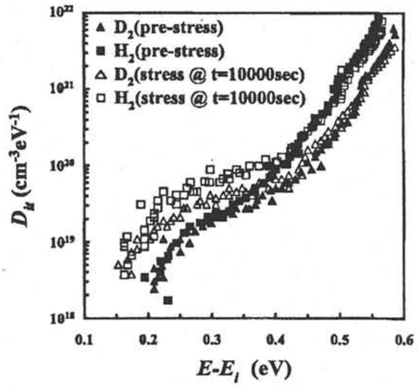

Fig. 3 Energy distribution of the density of states for devices before and after the stress.

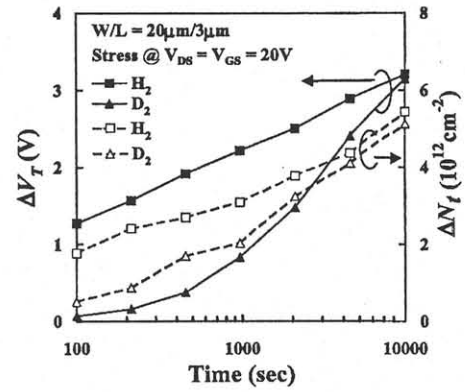

Fig. 6 Measured threshold voltage shift and trap state density (ΔN_t) for both stressed D_2 and H_2 devices.

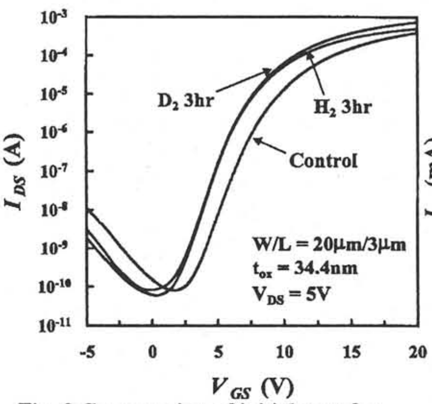

Fig. 2 Comparasion of initial transfer characteristics for LTP poly-Si TFT's with D_2 and H_2 passivation.

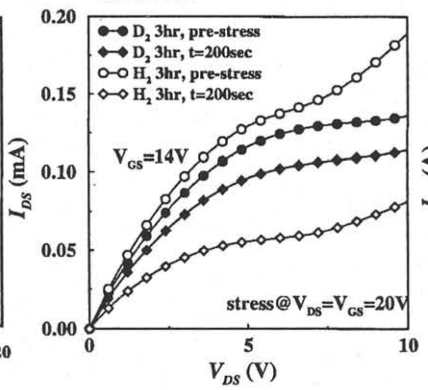

Fig. 4 Comparison of reverse-mode output characteristics with D_2 and H_2 passivation before and after the stress.

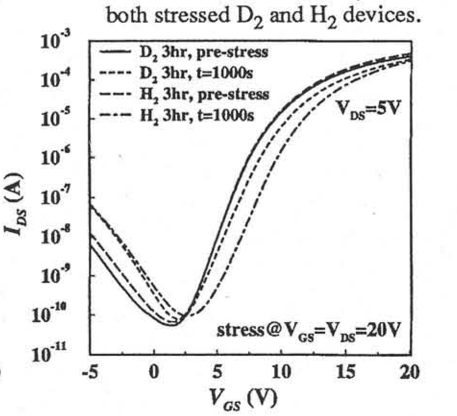

Fig. 7 Comparison of transfer characterics for poly-Si TFT's with D_2 and H_2 passivation before and after the stress.

	V_{th} (V)	Swing (V/dec)	I_{ON}/I_{OFF} ($\times10^6$)	μ_{FE} (cm^2/Vs)	N_t (cm^{-2})
Control	7.378	1.070	4.846	13.87	9.85×10^{12}
H_2 3hr	5.810	0.946	8.234	14.14	8.79×10^{12}
D_2 3hr	5.765	0.954	8.955	19.67	8.44×10^{12}

Table 1 Caculated device parameters of the poly-Si TFTs with D_2 and H_2 passivation.

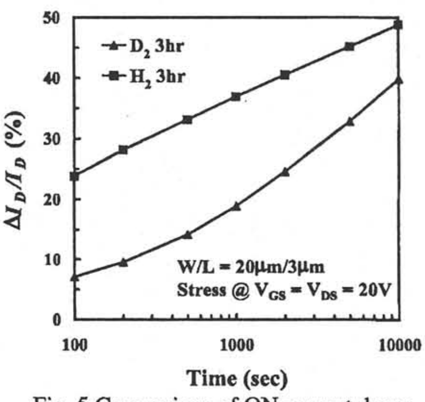

Fig. 5 Comparison of ON current degradation for both stressed D_2 and H_2 devices.

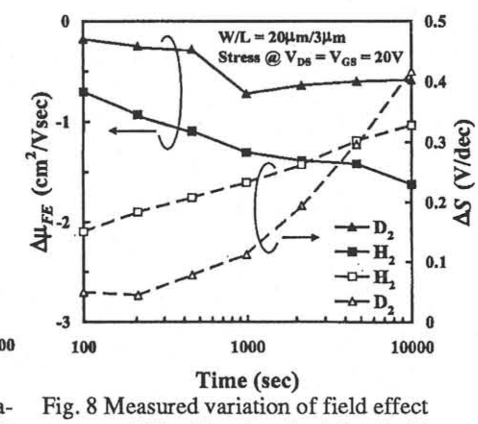

Fig. 8 Measured variation of field effect mobility ($\Delta\mu_{eff}$) and subthreshold swing (ΔS) for both stressed D_2 and H_2 devices.