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Two-Dimensional Numerical Simulation of Solid-Phase-Crystallized Polysilicon TFT Characteristics

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1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are actively studied by different laboratories for its potential use in the SRAM and large-area applications such as the active-matrix liquid crystal displays (AMLCDs) and x-ray image sensors. The main drawback of poly-Si TFTs in comparison with the crystalline silicon (c-Si) MOSFETs is the existence of the grain boundary states within the active region of poly-Si TFTs that can cause a lower field-effect mobility, a higher subthreshold slope and a higher leakage current. Thus, it becomes the most important issue to investigate how the grain boundary states at different interfaces affect the ON-state, subthreshold, and OFF-state characteristics in order to optimize the current-voltage behaviors of poly-Si TFTs.

2. Simulation Model and Experimental Results

In order to analyze the conduction mechanisms of poly-Si TFTs, there have been several models proposed by different authors[1]-[4]. However, those models neglect the poly-Si/gate oxide interface states (top grain boundary states) and the poly-Si/buffer oxide interface states (bottom grain boundary states), and they can be used to explain only the TFT ON-state or subthreshold behavior.

In this paper, we present a two-dimensional (2-D) numerical model that can explain the current-voltage characteristics of poly-Si TFTs. This model is based on DOS at the poly-Si/gate oxide interface, poly-Si/buffer oxide interface and inter-grain boundary (transverse grain boundary) as well as the low intra-grain defects. The energy distribution of DOS for all the defects is given by the commonly accepted double exponential expression (Fig. 1). A 1000Å thick n-channel poly-Si TFT prepared by solid-phase-crystallization (SPC) process with an average grain size of 0.5μm was used in this work (Fig. 2). The simulated characteristics (ON-state, subthreshold and OFF-state characteristics) of the poly-Si TFT show a very good agreement with the measured data as seen in Fig. 3 and Fig, 4.

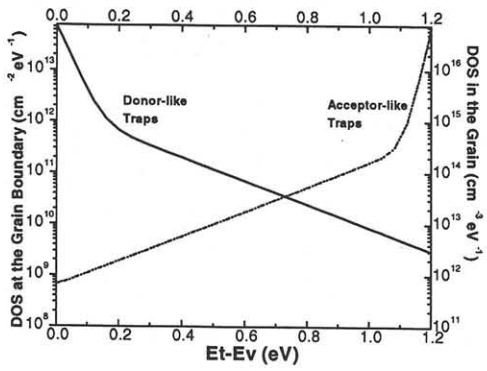

Fig. 1 Density-of-states (DOS) distribution at the grain boundary and in the grain used for 2-D simulation.

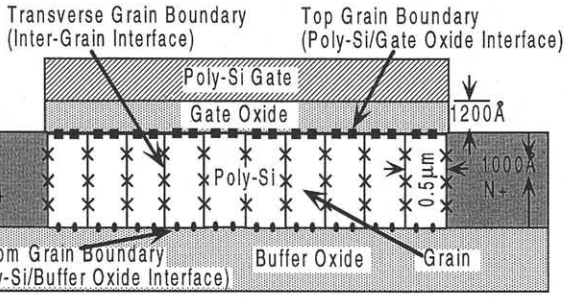

Fig. 2 Cross-section of 1000Å poly-Si TFT (not to scale) used in this modeling.

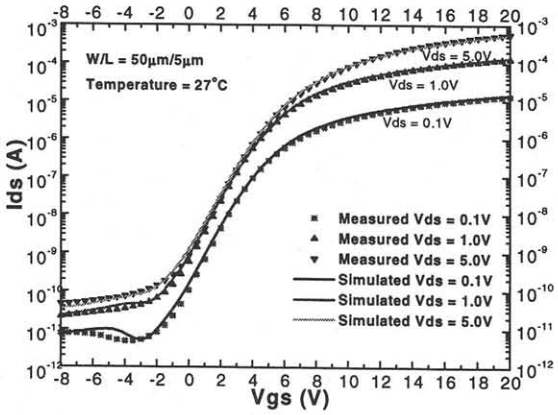

Fig. 3 Ids-Vgs characteristic of an n-channel poly-Si TFT. Markers are measured data. Lines are 2-D simulation results.

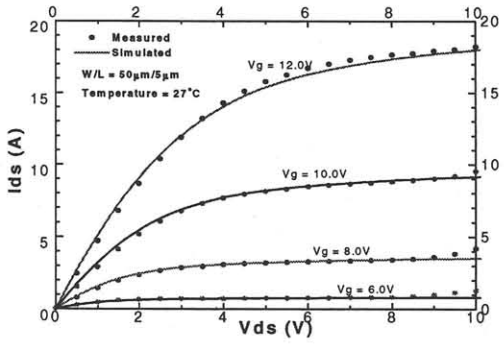

Fig. 4 Ids-Vds characteristic of an n-channel poly-Si TFT. Markers are measured data. Lines are 2-D simulation results.

3. Discussion and Analysis

In order to further investigate the importance of the grain boundaries at different interfaces, we simulated the characteristics of the poly-Si TFT by changing the DOS of the grain boundaries at different interfaces (Fig. 5, Fig. 6, and Fig. 7). The dimension of the poly-Si TFT is remained the same. The simulation results revealed that an increase of the poly-Si/gate oxide interface DOS causes a tremendous decrease of the ON- and subthreshold currents, thus, a reduction of the field-effect mobility and an increase of the subthreshold slope. The increase of poly-Si/gate oxide interface states also retards the onset of strong hole carrier accumulation in the channel region at negative Vgs bias, while the off-current is almost unaffected for Vds $\leq$ 5V. It is also demonstrated that the poly-Si/buffer oxide interface DOS has a small influence on the ON- and subthreshold currents. However, an increase of the poly-Si/buffer oxide interface traps can result in an increase of the OFF-current due to relatively larger density of the generation-recombination (G-R) centers created at the bottom interface near the drain region. Finally, we have established that the increase of the inter-grain boundary traps will result in not only a decrease of the ON- and subthreshold currents but also in an increase of the OFF-current.

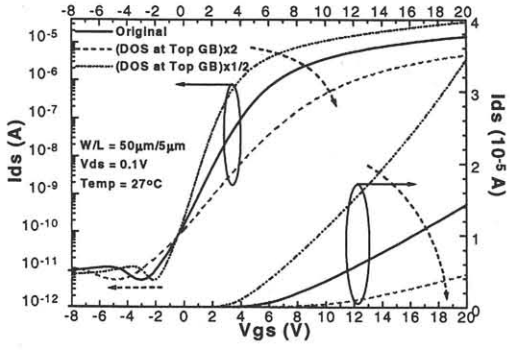

Fig. 5 Effect of DOS at the top grain boundary, i.e. the poly-Si/gate oxide interface, on poly-Si TFT characteristics.

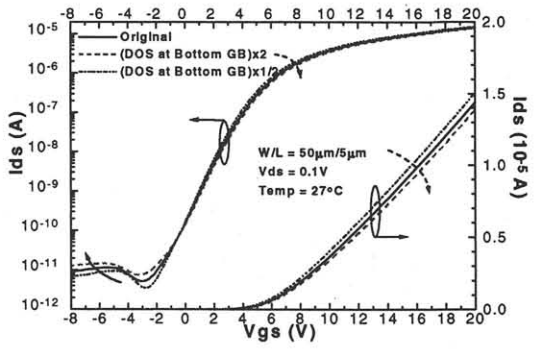

Fig. 6 Effect of DOS at the bottom grain boundary, i.e. the poly-Si/buffer oxide interface, on poly-Si TFT characteristics.

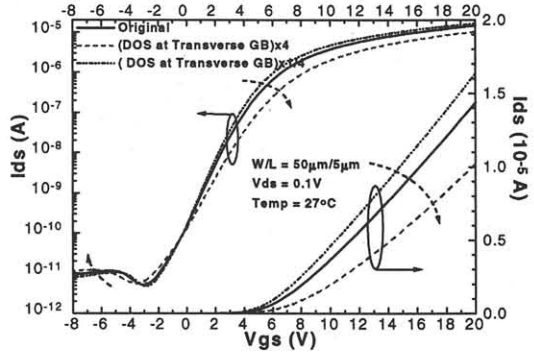

Fig. 7 Effect of DOS at the transverse grain boundary, i.e. the inter-grain interface, on poly-Si TFT characteristics.

4. Conclusions

For a 1000Å thick poly-Si TFT, it has been demonstrated: (i) ON-state and subthreshold behaviors of poly-Si TFTs can be mainly controlled by DOS at the poly-Si/gate oxide interface and inter-grain boundaries; and (ii) the OFF-state TFT behavior is dominated by the DOS at the inter-grain boundaries and poly-Si/buffer oxide interface. Thus, to improve the ON-state and subthreshold performance of poly-Si TFTs, it is necessary to reduce the poly-Si/gate oxide interface states and the inter-grain boundary states. The reduction of the inter-grain boundary states and the poly-Si/buffer oxide interface states will improve the OFF-state behavior of the poly-Si TFTs.

Acknowledgments

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References

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