Effect of Process Temperature on SiC MOS Properties

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1. Introduction

Oxide layers thermally grown on p-type SiC invariably exhibit high densities (6-7 x1011/cm2) of oxide charge, despite the gradual improvement over the years [1,2]. In contrast, the room temperature Jet-Vapor Deposition (JVD) process routinely gives rise to oxide charge densities on the order of mid-10¹⁰/cm² on p-type SiC [3] so long as the subsequent processing temperature does not exceed 950°C. Since we have had indications that a processing temperature higher than 1000°C could degrade the oxide quality, and thermal oxidation of SiC is typically executed at a minimum of 1025°C, we suspected that one major cause of the high oxide charge density in thermal oxide is its high processing temperature. In this study we used JVD oxide as a test vehicle to investigate the effect of processing temperature on the oxide charge density, with a goal of shedding some light on the origin of oxide charge in the thermal oxide on SiC.

2. JVD oxide on SiC

Jet Vapor Deposition is a room temperature process that utilizes a supersonic helium jet to carry reactive species rapidly to the substrate on which the film forms. The details of the JVD process may be found in [4, 5]. After the roomtemperature deposition, the JVD silicon dioxide film is typically given a two-step Post Deposition Anneal (PDA): 900°C in N₂ followed by 950°C Water Vapor Anneal (WVA), each one for 30min. The purpose of the first step is for film densification, and we suspect that the second step does two things: 1) slight oxidation of the deposited oxide film to make it more stoichiometric; 2) passivation of the carbon and silicon dangling bonds at the step edges of the off-axis cut SiC surface by atomic hydrogen and OH radicals in the water vapor. It is important to note that there is no oxidation of the SiC substrate at such a low temperature. Samples fabricated this way usually exhibit excellent electrical properties as exemplified by Fig. 1 and Fig. 2, and are used as the control in this study. To preserve the PDA temperature effect, no post-metal anneal was given after aluminum gate formation.

Figure 1shows the typical room-temperature photo-CV curves routinely obtainable on p-type 6H-SiC substrates. The corresponding oxide charge density is $6x10^{10}/cm^2$. Shown in the inset of Fig.1 is an enlarged portion of the CV

curve in depletion, on which a slight interface-state ledge is indicated [6], with a parallel section spanning the voltage interval between -2.6V to -3.1V. The voltage shift between these two curves is about 0.4V, which corresponds to a total density of interface states on the order of 4.4x10¹¹/cm². An example of high frequency C-V and G-V curves measured at 300°C can be found in [3], in which the oxide charge density was estimated to be 4.8x1010/cm2. Figure 2 shows the gate current density, measured in the temperature range of 27°C to 350°C, as a function of dielectric field. The leakage current density in the low-field region (below 6MV/cm) is always below 2x 10⁻⁸ A/cm², while in the high-field region it fits Fowler-Nordheim (F-N) tunneling model very well with a barrier height of 2.7eV. Similar to the case of oxide on silicon, the breakdown electric field of JVD oxide on SiC is slightly over 10MV/cm for oxides in the thickness range of 20-50 nm, and exceeds this value when the oxide is thinner.



Fig. 1, Typical high-frequency photo-CV curves of a SiC MOS capacitor made with JVD oxide as the gate dielectric.



Fig. 2, Current density, measured in a temperature range of 27°C to 350 °C, as a function of the dielectric field.

3. Degradation upon high temperature PDA

Compared to the thermal oxide on p-type SiC, the JVD oxide offers an order of magnitude reduction in oxide charge

density. Among many possible causes that made the difference, we suspected that a major one is the processing temperature. The lowest oxidation temperature is reportedly 1025°C [2], while the highest temperature involved in the JVD process is 950°C. To examine how the processing temperature would affect oxide properties, we did a set of experiments as described bellow: First, we deposit JVD oxide on 4 identical pieces of SiC substrates in the same run. Then, we treated these 4 pieces of samples with different PDA procedures, as summarized in Table I.

Table I. Summary of Post-Deposition-Annealing conditions used in this study, in which WVA stands for Water Vapor Anneal

Sample #	PDA condition
I (as control)	900°C N 2+ 950°C WVA
II	900°C N ₂ + 950°C WVA + <u>1050°C N₂</u>
III	<u>1050°C N₂ + 950°C WVA</u>
IV	900°C N ₂ + <u>1050°C WVA</u>

In table I, sample 1 serves as the control in this study, which received the standard two-step PDA. Sample 2 was given an additional N₂ anneal at 1050°C, and severe degradation was observed as depicted by curve II in Fig.3. It is apparent that the 1050°C N₂ annealing caused as much as -4V of flatband voltage shift, which corresponds to an increase of 4×10^{12} /cm² in oxide charge. There is also a substantial widening of the hysteresis window, indicating a significant increase in interface traps. A significant degradation is also observed in sample 3, for which the nitrogen annealing temperature was increased from 900°C to 1050°C, while the other processing



Fig.3, CV curves corresponding to the PDA conditions in Table I

parameters were unchanged from the control sample. This is shown by curve III in Fig.3. The PDA conditions for sample 4 in table I is very similar to that used for wet oxidation of SiC at the Cree Research Inc, except that there is a JVD oxide layer on top of the SiC substrate in our case. However, the JVD oxide layer cannot prevent wet oxidation of the SiC surface at such a temperature.

An examination of the data in Fig.3 reveals a clear trend: any processing temperature that is sufficiently high to cause oxidation of the SiC surface will result in a high density of oxide charge. In the case of samples 2 and 3, the 1050° C N₂ annealing drives the oxidation of SiC by the oxidants embedded in the deposited SiO₂, while in the case of sample 4 the 1050° C WVA step is the obvious culprit.

It should be noted that the experiments described in Table I have been carried out several times, and the results on p-type SiC are very repeatable, self-consistent, and therefore conclusive.

The reason that high-temperature oxidation results in poor oxide and interface quality, we believe, is that thermal oxidation requires the breakage of Si-C bonds, and the subsequent oxidation tends to occur preferentially at the Si sites, leaving behind the carbon dangling bonds which may be responsible for the increase in the oxide charge density. At higher temperatures, depassivation of previously hydrogen-passivated dangling bonds (which could be formed during previous PDA) may also take place. In fact, it is reasonable to assume that depassivation and oxidation occur simultaneously. This may explain why accompanying the flatband voltage shift, there is always a widening of the hysteresis window.

4. Conclusion

We have demonstrated that the process temperature could significantly affect the quality of the oxide/SiC interface. In particular, our results strongly suggest that a process temperature sufficiently high as to cause thermal oxidation of the SiC surface will lead to a high density of oxide charge. If this is true, then the thermal oxidation process is bound to give rise to high densities of positive oxide charge. Therefore, thermal SiO₂ may have to be replaced by a deposited oxide eventually. Even in the case of deposited oxides, our study suggests that avoiding oxidation of the SiC substrate during the entire process may be the key to realizing a high quality SiO₂/SiC interface. These results are all based on p-type SiC, and we plan to do a systematic investigation of the process temperature dependence on ntype SiC substrates in the near future.

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