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Single-Electron Tunneling in Nanocrystalline Silicon

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The development of silicon integrated circuits has been put forward by miniaturization using advanced lithography technologies. According to the technology roadmap[1], this tendency will continue until 2010, when the design rule becomes 50nm and 64Gbit DRAM is projected. Further miniaturization will lead to problems of increased leakage current due to quantum mechanical tunneling effect, and that of quantum noise, or fluctuation of device characteristics since only a few electrons participate in device operation. In nanoscale devices, it is essential to control quantum effects. Tunneling phenomena should be suppressed, for example, by means of Coulomb blockade effect[2], which provides a novel device principle suitable for a situation having only a few electrons. A paradigm shift is also required for the method of nanostructure fabrication. Lithography may no longer be the unique method for the fabrication of nanostructures uniformly and economically. Self-organized systems employing the basic understanding of the nature of crystal growth are emerging instead. As for materials, compound semiconductors have been widely investigated for quantum effect devices. However, silicon is preferable on the basis of accumulated knowledge of process technologies.

Researchers at Hitachi have successfully observed single electron tunneling characteristics at room temperature from devices made of polycrystalline silicon[3]. They also demonstrated operation of single-electron memory integrated circuits[4,5] using the same material.

However, issues such as synthesis of silicon quantum dots with a precise control of size, position and interface states remain critical, thus we have investigated fabrication of nanocrystalline silicon (nc-Si) using plasma processes and observed single electron tunneling characteristics.

Nanocrystalline silicon quantum dot structures with size less than 10nm and a very small spread of size (1nm) have been fabricated by very-high-frequency (144MHz) plasma decomposition of silane and coalescence of radicals[6-8]. The principle idea for the formation of uniform structure is the separation of the nucleation and the crystal growth processes. We have introduced into a silane plasma a hydrogen gas pulse that enhances the nucleation of nc-Si particles. The nuclei grow in size in the silane plasma during the off state of hydrogen gas supply. The next hydrogen gas pulse forces nc-Si particles grown in the previous cycle out of the plasma cell into the deposition chamber and the next nucleation of nc-Si occurs simultaneously. The growth rate is also enhanced by increasing plasma excitation power, pressure and use of an Ar dilution gas.

Nanocrystalline silicon particles can be deposited at room temperature onto many kinds of substrate such as carbon microgrids for TEM measurements, quartz for photoluminescence measurements [9] and thermal oxidized silicon with patterned polycrystalline silicon electrodes for electrical measurements.

Natural oxide which covers the surface of nc-Si plays very important roles in the characteristics of nc-Si. First, the oxide serves as a potential barrier which controls charge, energy quantization, and tunneling current. Second, the oxide passivates the surface dangling bonds resulting in reduction of electron traps and enhancement of luminescence efficiency. Third, the oxide serves as glue for nc-Si to fix to the substrates. Further reduction of nc-Si dot size can be implemented by oxidation and etching in oxygen with various pressures and temperatures.

Although nc-Si particles distribute randomly, electrodes patterned by EB lithography can be designed such that nc-Si position is not critical. In addition, the position of nc-Si particles can be manipulated by AFM tip while observing the image. We have also found that nc-Si particles are deposited preferentially at the steps of substrate surfaces[8].

Electrical properties of a single dot [10] and an array of multiple dots of nc-Si were evaluated[11]. Electron beam lithography with RD2000N negative resist and dose correction technique for proximity effect reduction followed by ECR reactive ion etching made possible formation of SOI layer electrodes having separation between 10-20nm. Nanocrystalline

silicon dots were deposited by the plasma process onto the electrodes and coated by a PECVD SiO_2 film. The electrodes were doped to $10^{19}cm^{-3}$ by ion-implantation. Top gate electrode was prepared with gate oxide thickness of 20nm. Coulomb blockade of as large as 0.9V was observed in I-V characteristics measured at various temperatures. Zero point shift found in I-V characteristics may be due to the background charges. A small Coulomb island and multiple tunnel junction structure were fabricated by EB processes. A hysteresis was observed in I-V characteristics, suggesting multiple transport path and can be applied to memory devices.

In order to avoid complexity associated with multiple dots, we measured transport properties of individual surface oxidized nc-Si particles. The measurements were performed using AFM with conductive tips in air at room temperature[10]. The grain size and the position of the nc-Si were directly observed by AFM. The measured I-V characteristics show staircaselike features. The period of the staircase increases with decreasing nc-Si grain size, which is consistent with a single electron charging effect in the nc-Si. Since the AFM measurement is not possible at low temperatures and exposure to ambient results in stability problem, we prepared samples having nanoscale holes in oxide on Si substrates and deposited nc-Si particles in the holes. Polysilicon electrode was coated on top of the nc-Si dots. The current suppression due to Coulomb blockade was observed in I-V curves of these samples.

These results suggest that single electron tunneling devices based on silicon quantum dots are promising for future ultralarge scale integrated circuits.

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