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Gated Resonant Tunneling Structures with Buried Tungsten Grating Adjacent to Semiconductor Heterostructures

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1. Introduction

Laterally modified potential structures on the nanometer scale are promising for the realization of electron wave devices based on the control of the wave properties such as interference and/or diffraction. A coherent electron wave device was proposed by using an ultra-fine grating structure buried in semiconductors, in which a wavefront of ballistic hot electron is modified[1].

Recently, a fabrication technique for definition of ultra-fine tungsten (W) structures in semiconductors has been established by electron beam lithography (EBL) and overgrowth by metal organic vapor phase exitaxy (MOVPE) [2]. By using this technique, nm-size W disks combined with GaInP/GaAs resonant tunneling diodes (RTDs) were fabricated and possibility of constricting the vertical current flow through an opening in the disk lattice were investigated[3].

In this paper, fabrication and characterization of gated GaInP/GaAs resonant tunneling structures with a buried W-grating is reported for the first time. A possibility to modify the lateral size of the channel due to gate bias is investigated. The fabrication of the gated RTD structure presented in this paper is different from the previously reported ones[4-6] since we can define the spacing between the metal and the heterostructure in a controlled way by the epitaxial growth.

2. Fabrication

The fabricated device structure is schematically shown in Fig.1. Electrons are emitted through GaInP/GaAs double barrier RTD toward a mesa top. A 20-nm-thick W-grating was buried in the collector side of the RTD, with a 30-nm-thick spacer layer between the metal and the semiconductor barrier. Both linewidth and spacing of the grating were 125 nm to attain successful buried growth with good Schottky junction. A window with 1.4×1.4 μm^2 side-length was formed in the grating to laterally define a vertical current channel for electrons emitted from the tunneling barrier.

All semiconductor layers were grown by MOVPE on n^+-GaAs (001) substrate. In the first growth, active layers of the GaInP/GaAs RTD were fabricated with a 100-nm-thick n-GaAs emitter, a 20-nm-thick i-GaAs spacer, a 3 nm i-$Ga_{0.5}In_{0.5}P$ barrier, a 9-nm-thick i-GaAs quantum well, a 3-nm -thick i-$Ga_{0.5}In_{0.5}P$ barrier, a 20 nm i-GaAs spacer and a 10-nm-thick n-GaAs cap layer. All thicknesses are nominal values.

After the first growth, a 20-nm-thick W pattern consisting of the fine W-wires and 40×40 μm^2 large pads for gate contact were simultaneously defined using EBL on double layer PMMA and lift-off[7]. Figure 2 shows a SEM-image of the opening channel on the W-grating prior to the overgrowth. In order to embed the W-grating and to planarize the regrown surface, the W-grating was oriented at 60° from the [110] direction [7].

An overgrowth was performed with 600-nm-thick n-GaAs layer and highly doped n^+-GaAs cap layer. During the overgrowth, a GaAs mesa structure was selectively formed over the 40×40 μm^2 grating region. The doping concentration for n-GaAs layers was selected as 8.0×10^{16} cm^{-3} which provides electrons with 20 meV of the Fermi level above the conduction band edge. After the growth, Ge/Au/Ni/Au ohmic contacts were defined on top of the mesa and to the back side of the substrate.

According to a theoretical calculation of the potential profile in the GaAs in between the W-wires, an effective channel for vertical current is present inside the opening with depleted regions around the Shottky junction when the gate voltage is zero.

3. Measurements

Samples were characterized at 20 K using a probe station. Measured collector current, I_c, v.s. emitter-collector voltage, V_{ce} (>0), in a gated GaInP/GaAs RTD is shown in Fig.3 for various gate voltages, V_g. Under these conditions, electrons were flowing from the substrate towards the mesa top. As shown in Fig.3, the peak current decreased with increasing absolute value of V_g(<0) and the main current peak revealed several sub-peaks for different V_{ce}. The variation of the effective channel area can be evaluated by comparing the current level with large area RTDs. It was found that the effective area was reduced by a factor of 0.6 when V_g was changed by 3 V.

The differential conductance around the main peak in Fig.3 showed several conductance minima. These fine features were slightly modified by V_g as expected. Quantization of lateral motion of electrons in the channel is believed to contribute to the fine feature, since the energy splitting is in the same order as what is estimated using a simple potential model. However, at present we can not exclude other options, such as inhomogenieties in the double

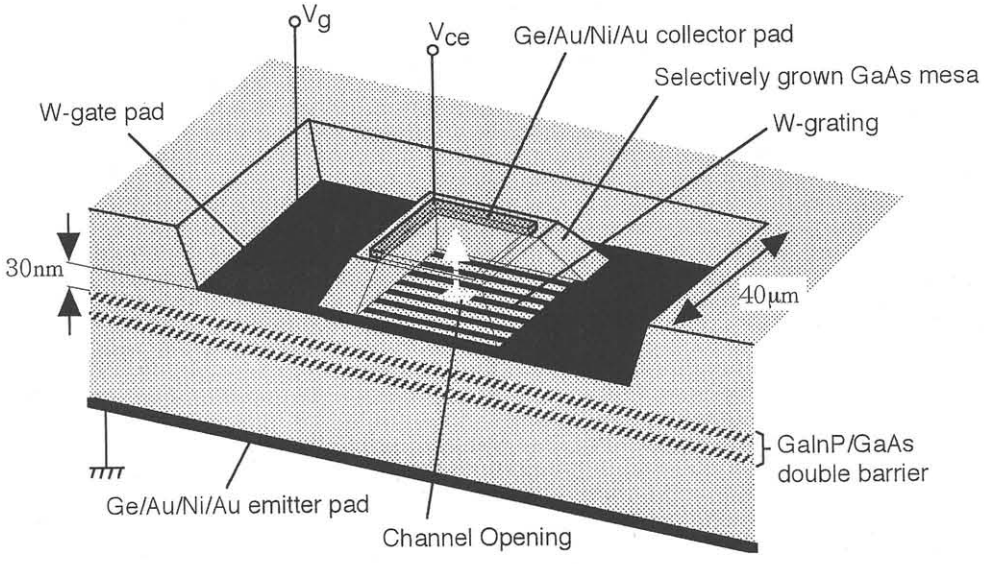

Fig.1 Schematic view of the device structure. During the MOVPE regrowth, the W-grating was buried and a GaAs mesa structure was formed over the grating.

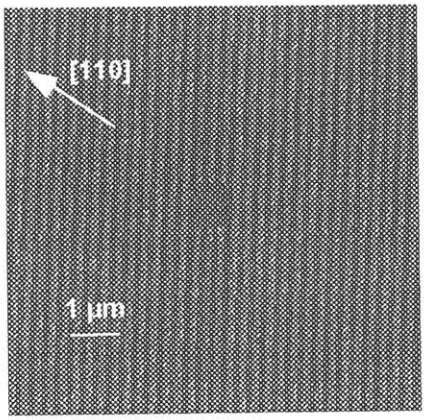

Fig.2 SEM view of the channel opening in the W-grating.

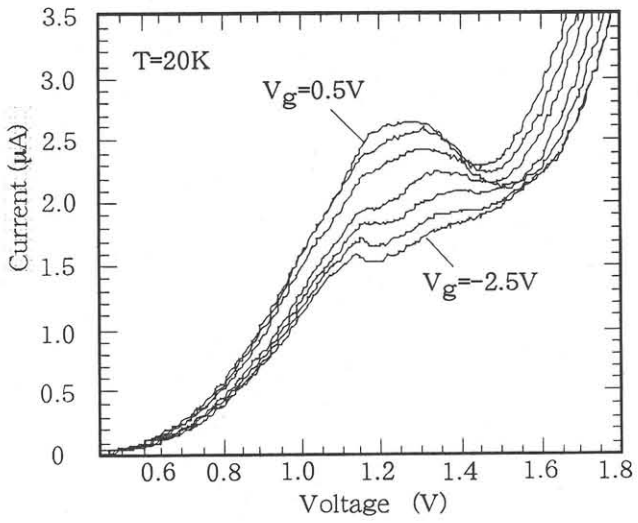

Fig.3 Measured collector current v.s. emitter-collector voltage characteristics for various gate voltage. V_g is changed in steps of 0.5V. An opening window with 1.4×1.4 μm^2 square was formed in the W-grating on the sample, defining the current channel.

barrier structure.

4. Conclusions

To demonstrate the control of the potential properties with fine metals buried in semiconductor nano-devices, a W-grating was integrated as a control gate in RTDs. MOVPE grown GaInP/GaAs RTDs gated by the embedded W-grating with a 1.4×1.4 μm^2 opening were characterized at 20K. Several fine features were observed directly in the current-voltage characteristics and the differential conductance in addition to a typical negative resistance property of RTDs. The fine features as well as the peak to valley current ratio were modified by the gate bias. It suggests that the W-grating buried in semiconductors is useful to control transport properties in nano-devices.

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