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STM Nano-Lithography with SiO_2 Mask

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1. Introduction

Nano-fabrication has attracted increasing interests in recently because of its great potential to the development of science and technology in the next century. With fine focused high energy electrons such as employed in TEM or SEM [1,2], an e-beam stimulated etching of the SiO_2/Si surface has been demonstrated with which nano-meter sized windows were cut through the SiO_2 overlayer and subsequent growth of the nano-dots was fulfilled [3].

Besides the high energy e-beam induced surface reactions, Electron Stimulated Desorption (ESD) has been widely studied in surface analyses and that shows the energy required to induce dissociation of various molecules from material surfaces can be down to several tens to hundreds eV [4, 5]. This suggests a possibility of using low energy electron to stimulate a reaction on the SiO_2/Si surface to conduct a nano-fabrication.

SiO_2 is such an important material which is closely related to the silicon industry. It is stable, durable, and reliable, and thus directly involved in the fabrication of electronic devices. Using SiO_2 as a mask for nano-fabrication/lithography may take all those advantages of the silicon industry related to formation of the SiO_2 overlayer, and may simplify the traditional lithography techniques.

The aim of this study is to investigate the possibility of conducting a low energy electron stimulated reaction on the SiO_2/Si surface by using STM, for the purpose of initiating a new method for nano-fabrications. Our results show that both the low energy electron stimulated reaction (simplified as LEESR below) on the SiO_2/Si surface and employing STM as the tool to perform such a selective etching can be convinced. The LEESR process also provides us a new possibility to diagnose the SiO_2/Si interfaces with STM.

2. Experimental

Our experiments were carried out with a commercial UHV STM system (JSTM-4610X from JEOL). Both thermal and native Si oxide were used in the study. The samples were cut from an n-type Si wafer with (001) orientation. Tungsten tip was used in the STM processing and imaging, which was cleaned with e-beam bombardment and field evaporation. The thermal oxide on top of a clean Si substrate was formed in the UHV chamber by dosing O_2 at a pressure of ~2.0 x 10^{-4} Pa, while the surface was heated at ~700 °C. After oxidation, it was observed by STM that the SiO_2/Si surface is rough with SiC microcrystals but basically uniform, indicating a good quality of the oxide layer on top of the Si surface. By the STM image after the e-beam processing, the thickness of the SiO_2 overlayer is estimated to be about 0.5 nm with 600 L of oxygen exposure. For native Si oxide sample, it was only degassed at an intermediate temperature for a few hours before a LEESR/STM processing.

3. Results and discussions

A typical result of the LEESR/STM processing can be illustrated by the STM image shown in Fig. 1. The etching was performed at a bias voltage of 150 V and field emission current of 50 nA. In Fig. 1(a), a clear contrast change within the round area at the center of the image can

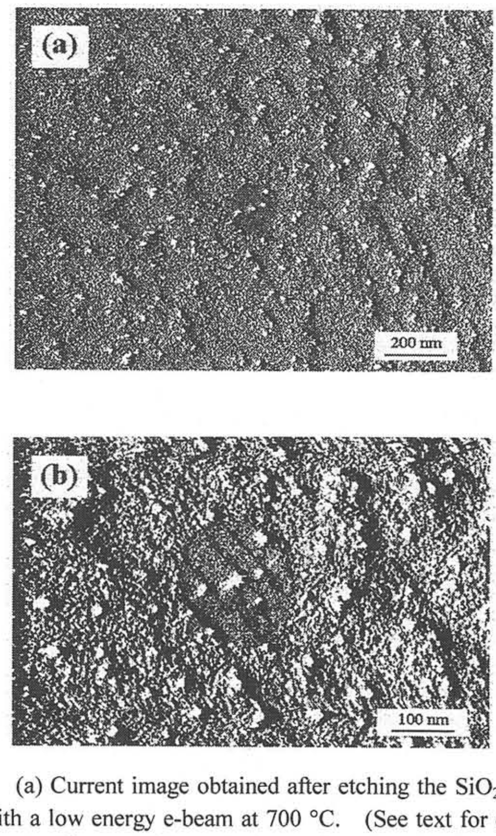

Fig. 1 (a) Current image obtained after etching the SiO_2/Si surface with a low energy e-beam at 700 °C. (See text for details.) (b) A zoomed image of the etched area shown in (a).

be seen, where the surface was irradiated by the low energy e-beam. Also the current fluctuation in this area is apparently reduced. This result confirms that a surface reaction occurred around the area exposed to the low energy e-beam. The clear atomic steps of the Si substrate within the processed area, as can be seen in the zoomed image of Fig. 1(b), indicate explicitly an evacuation of the SiO_2 layer and suggest formation of a clean surface in this area. By selecting the bias voltage, emission current, and exposure time, different sizes of the etched SiO_2 windows down to a nanometer scale can be obtained with the e-beam stimulated reaction. This result demonstrates evidently the possibility of etching the SiO_2 coating layer with the LEESR, and that to conduct such a processing with the scanning probe, STM. Besides, this result also presents a possibility to diagnose the SiO_2/Si interface buried below the SiO_2 top layer by this LEESR/STM method.

In Fig. 2(a) an STM image on fabricating an array of nanometer sized windows on a native SiO_2/Si surface with the LEESR/STM processing is shown. The fabrication was performed at an e-beam energy of 55 eV and beam current of ~ 10 nA. During the processing, the tip position was changed by manually moving the scanning offset of the STM. The beam current and exposure time were also set manually, so that these parameters could not be

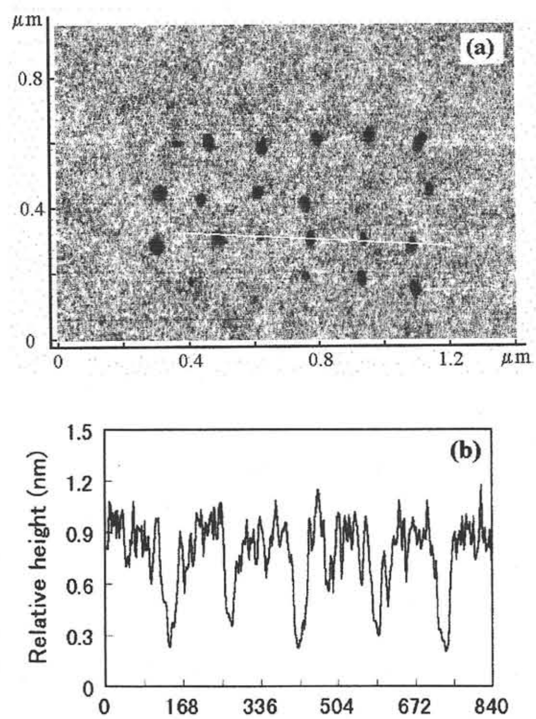

Fig. 4 **(a)** STM image of a window array etched through the SiO_2 overlayer on top of a Si substrate. (See text for details.) **(b)** Cursor plot across the line as shown in (a).

controlled precisely, and the positions and sizes of the cut windows have a fluctuation. Even so, the size of the formed windows on the SiO_2/Si surface falls into a range of 25 nm to 65 nm. By the cursor plot across a few of the cut windows, as shown in Fig. 2(b), the depth of the windows, or, the thickness of the SiO_2 overlayer, can be estimated to be ~ 0.65 nm. In our experiment, window depth up to 3 nm can be obtained. These results show also the capability of the LEESR/STM processing technique.

At present, the mechanism dominating the LEESR process is still not very clear. We suppose that it can be related to a low energy electron induced surface reaction followed by thermal desorption of SiO, similar to that in the case of a high energy e-beam stimulated reaction[1]. It is unlikely that electrical field effects or direct e-beam heating dominates the process, from different results we obtained until now. More detailed studies should be conducted to make clear of the mechanism for the LEESR process.

4. Summary

We have performed an experimental study on the low energy electron stimulated reaction on the SiO_2/Si surface by using STM. It is shown that with a low energy (50 - 160 eV) e-beam irradiation followed with a thermal treatment, SiO_2 on top of a Si substrate can be evacuated and windows down to 25 nm can be formed. These results demonstrate evidently the possibility of fabricating the SiO_2/Si surface by the LEESR/STM processing, and show the capability in nano-fabrication and possibility for diagnosing the SiO_2/Si interface of this method.

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