Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 72-73

Fabrication of High-Resolution and High-Aspect-Ratio Patterning on a Stepped Substrate by Scanning Probe Lithography Using a Multilayer-Resist System

Masayoshi Ishibashi, Nami Sugita, Seiji Heike, Hiroshi Kajiyama, and Tomihiro Hashizume

Advanced Research Laboratory, Hitachi, Ltd.
Hatoyama, Saitama 350-0395, Japan
Phone +81-492-6111, Fax: +81-492-96-6006, E-mail: isibasi@harl.hitachi.co.jp

1. Introduction

Nanofabrication techniques are indispensable for fabricating promising devices. Scanning probe lithography (SPL), which is based on scanning tunneling microscopy (STM) or atomic force microscopy (AFM), is an effective method of fabricating nanoscale structures[1]. In a previous paper, we reported some of the advantages of AFM-based lithography using a constant-current-controlled exposure system, they include high resolution, low variation in the linewidth of the pattern and a negligible proximity effect[2]. Scanning probe lithography has the following disadvantages, however;

1. A thin-resist film is required to fabricate small patterns since the resolution depends on the thickness of the resist.
2. Topography or existing steps on the surface cause deviation from the designed pattern .
3. Resist patterns cannot be formed on insulating surfaces.

Multilayer-resist systems [3], which have been used in optical lithography and electron-beam lithography to avoid the standing-wave and proximity effect, are an effective solution to these problems. K. Kragler et al. fabricated 100-nm-wide resist patterns, 300 nm thick by STM lithography using a bilayer-resist system consisting of silicon-containing positive resist and amorphous hydrogenated carbon[4].

In this report, we describe how we used a trilayer-resist system to fabricate high-aspect-ratio and high-resolution resist patterns on a stepped substrate using current-controlled AFM lithography.

2. Experimental

A commercial contact-mode AFM system was used to control the tip position. A tip was coated with 20-40 nm of Ti. The system had a second feedback system to adjust the negative-bias voltage applied to the Ti-coating tip in order to keep the field emission current constant[2],[5]. The current was 10-100 pA, and the scanning speed of the tip was 0.05-0.1 mm/s.

The process flow of the trilayer resist system using SPL is shown in Fig. 1. The trilayer resist was coated on a 150-200-nm-stepped Si substrate. We used 300-nm BLOC (Hitachi Chemical Co.) as a bottom-planarizing layer, 30-nm sputtered Si as an intermediate-conductive layer, and 40-nm RD2100N negative-type resist (Hitachi Chemical Co.) as a top-imaging layer. The top layer was exposed by applying a bias voltage between the tip and intermediate layer. After exposure, the imaging layer was developed using an alkali developer. The patterns of the top layer were transferred to the intermediate layer by reactive ion etching (RIE) using CF_4, and the patterns of the intermediate layer were transferred to the bottom layer by RIE using O_2. The resist and the developer in the single-layer resist system were the same as those used for imaging layer in the trilayer resist system.

3. Results and discussion

The AFM cross-sectional profiles of a 150-nm-stepped surface before and after being coated with 40-nm single-layer resist are shown in Figs. 2(a) and 2(b), respectively. The height of the surface remained 100 nm after it was coated. The designed and formed resist patterns on the 150-nm-stepped surface using a single-layer resist system are shown in Figs. 3(a) and 3(b), respectively. The patterns were not formed near the step and the parts of the step were destroyed. Apparently the tip hit the front of the step, since the vertical-position could not be controlled by the AFM feedback. The top of tip, which has a 50-nm radius, therefore could not reach near the step due to the hindrance

The AFM cross-sectional profiles of a 200-nm-stepped surface before and after being coated with the bottom layer are shown in Figs. 4(a) and 4(b), respectively. The step was planarized by the bottom layer. As shown in Fig. 5, line-and-space resist patterns were fabricated on the 200-nm-stepped surface by the trilayer-resist system. The linewidth and aspect ratio were about 50 nm and 7, respectively. It is

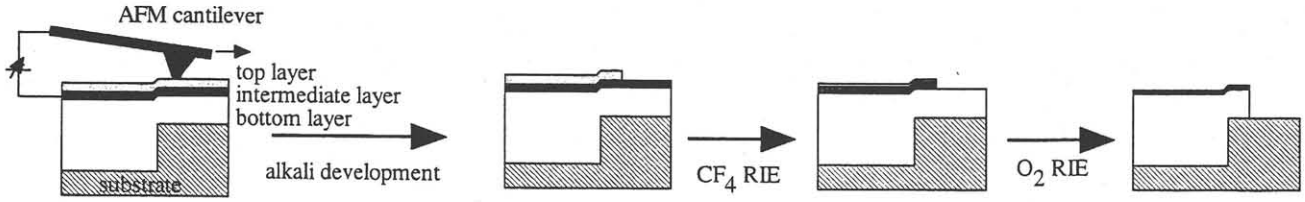

Fig. 1 Process flow of trilayer-resist system using AFM lithography.

also possible to fabricate a resist pattern on an insulating surface by this method because the bias voltage for exposing the resist can be applied between the tip and the conductive intermediate layer.

4. Conclusion

We successfully fabricated 50-nm-wide line-and-space resist patterns, 340 nm thick, on a 200-nm-stepped substrate by current-controlled AFM lithography using a trilayer-resist system. This method also makes it possible to fabricate patterns on an insulating surface.

We would like to thank Dr. Yasuo Wada for valuable discussion.

References

1. M. A. McCord, and R. F. W. Pease: J. Vac. Sci. Technol. **B4** (1986) 86.
2. M. Ishibashi, S. Heike, H. Kajiyama, Y. Wada, and T. Hashizume: Appl. Phys. Lett. **72** (1998) 1581.
3. M. Hatzakis: Solid State Technol. (1981) 74.
4. K. Kragler, E. Gunther, R. Leuschner, G. Falk, A. Hammershmidt, H. von Seggen, and G. Saemann-Ischenko: Appl. Phys. Lett. **67** (19958) 1163.
5. K. Wilder, H. T. Soh, A. Atalar, and C. F. Quate: J. Vac. Sci. Technol. **B15** (1987) 1811.

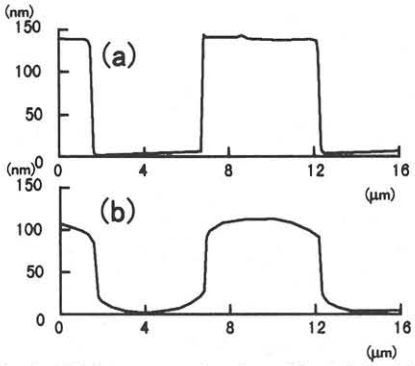

Fig. 2 AFM cross-sectional profiles of the 150-nm-stepped surface (a) before and (b) after being coated with a 40-nm single-layer resist.

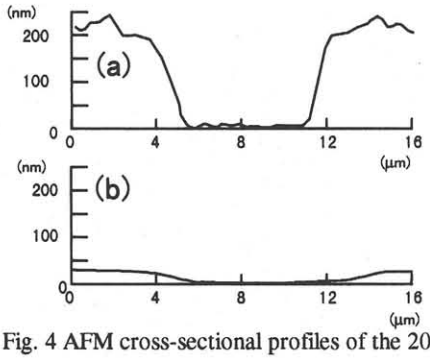

Fig. 4 AFM cross-sectional profiles of the 200-nm-stepped surface (a) before and (b) after being coated with the bottom layer.

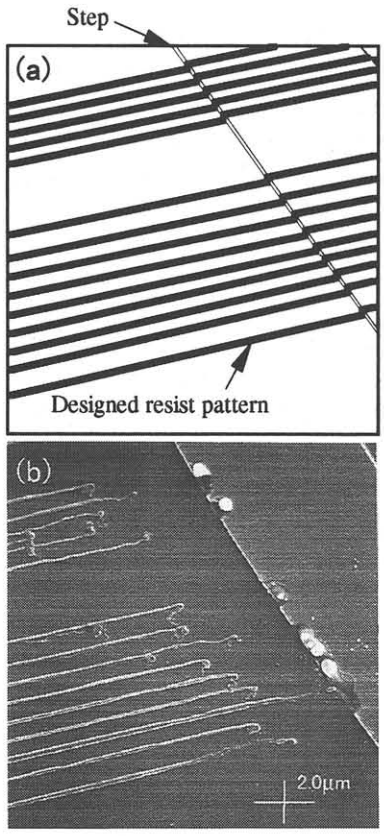

Fig. 3 (a) Designed and (b) formed resist patterns on the 150-nm-stepped surface with a single-layer resist system.

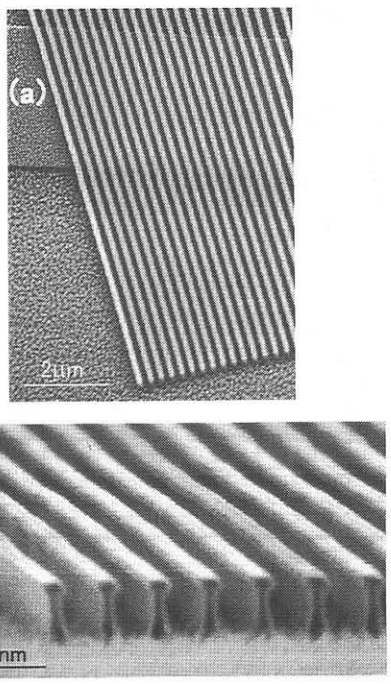

Fig. 5 SEM micrographs of line and space resist pattern fabricated on a 200-nm-stepped surface by a trilayer-resist system.