Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 168-169

Invited

Nano-Crystal and Quantum Dot Memories: Device Properties

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1 Introduction

Nano-crystal and quantum-dot memories [1-5] are flash memory structures (Fig.1 and 2) where the storage floating gate has been

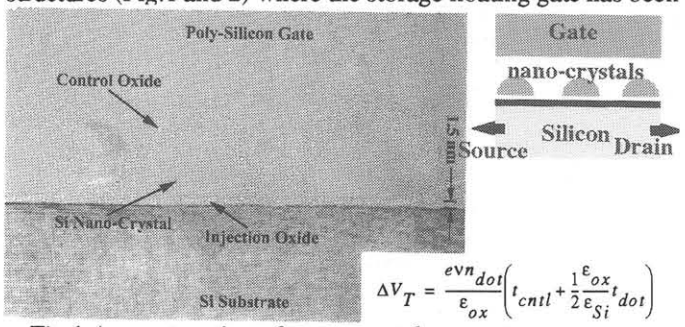

Fig.1 A cross-section of nano-crystal memory.

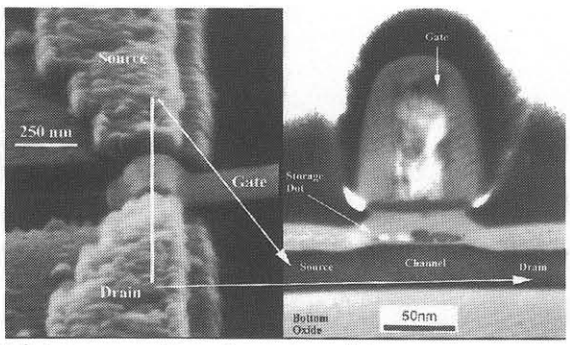

Fig.2 A cross-section of quantum-dot memory.

scaled to dimensions that make quantum-confinement and single electron effects significant. While maintaining this sensitivity to single electrons trapped in small capacitance silicon islands, a large threshold voltage and conductivity shift is obtained at low voltages and is observable in currents ranging from nA to μA for small devices, and with appropriate change in the design of the quantum-dot-containing gate-stack, refreshing ranging from seconds to non-volatility can be obtained.

2 Device Structures and Properties

These quantum-dot(s) based memory structures consume low power, operate at logic compatible voltage, and employ CMOS-compatible processes, and hence are interesting alternatives to DRAMs and E^2PROMS. For the former, the advantage is in the simplicity and scalability to small dimensions. For the latter, the advantage is in the low power, higher speed and smaller dimensions. The major disadvantage for the former is in the speed reduction by factors of 10 or more and, for the latter, is in a change in technology and architecture. As device dimensions continue to shrink, device structures such as these are of increasing interest for their CMOS-compatible simplicity, and their adaptability to applications - from embedded to high density memory - requiring coexistence of logic and memory on the same silicon substrate. Use of small dimensions, however, comes with some additional technology demands beyond that of CMOS: (a) a control of small dimensions for the silicon islands near 5 nm so that the threshold voltage shift and its variance with multi-electron storage is small (see Fig.3), (b) small injection

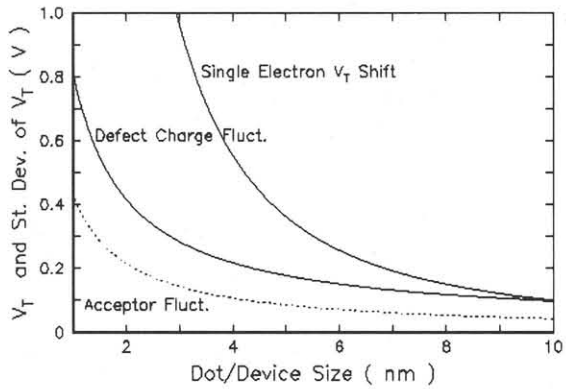

Fig. 3 Single electron threshold-voltage shift together with shift due to defect charge fluctuation and the fluctuation in acceptor charge.

oxide thicknesses (<3 nm) to allow direct tunneling, and (c) good interface state density control of control oxides and dot/thermal oxide interface to control defect sensitivity. As seen in Fig. 3, a reasonable operating voltage range is obtained when the quantum-dot dimensions are close to 5 nm and multiple electrons are stored in the quantum-dots to make the device defect insensitive. Conventional flash structures usually employ a large oxide thickness in order to reduce the leakage of charge, and in turn, have to employ injection mechanisms based on either hot carriers or high local electric fields to obtain small write times that are typically ms's. A significant departure in the design of these structures is an attempt to provide efficient coupling to inversion layer (through short oxide distances), but not to the contact regions (through long oxide distances). The nano-crystal density (~10^{12} cm^{-2}) and nano-crystal to nano-crystal spacing (>5 nm) discourages degradation both due to oxide defects and to the doped contact region of field-effect structures. If an electron leaks from one of the nano-crystals, the surrounding nano-crystals can still contribute to blocking of conduction. Nano-crystals on the doped access regions of source and drain can leak easily because of the reversibility of tunneling, but the ones on the effective channel do not, because of differences in lifetime between a write and erase or read cycle. This interesting com-

parison with non-volatile structures is exemplified in Fig. 4 which shows a nano-crystal memory's hysteresis characteristics with 3.0 nm tunneling oxide thickness. This attribute of tunnel-

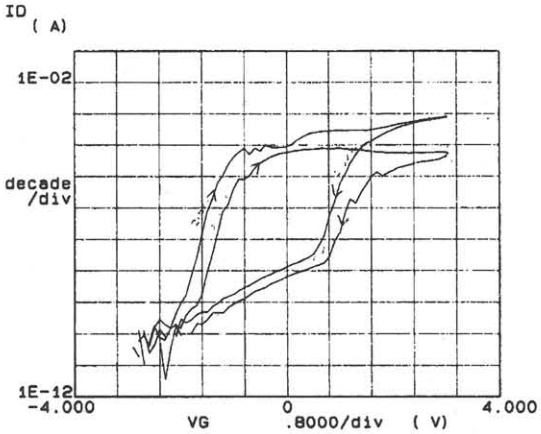

Fig. 4 An example of ~5 electrons per nano-crystal storage in a nano-crystal memory with 3.5 V biasing.

ing shows quite clearly in tunneling in thin oxide (similar to the injection oxides) of field-effect transistors. Fig. 5 shows a cross-section, extracted tunneling currents in the fabricated devices, and calculated tunneling currents from accumulation and inversion layer. The response time - write and refresh - is summarized

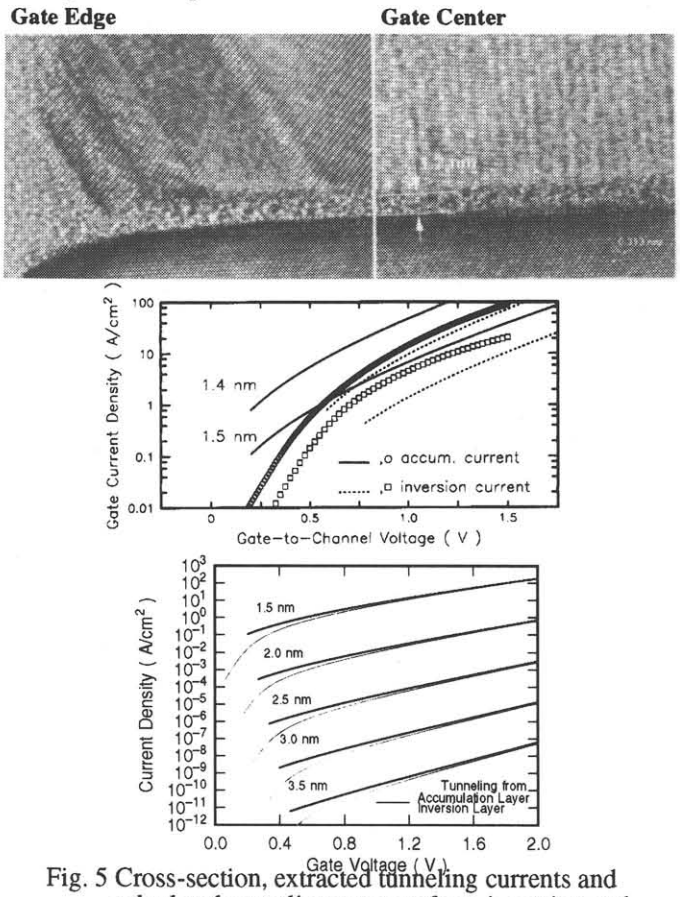

Fig. 5 Cross-section, extracted tunneling currents and calculated tunneling currents from inversion and accumulation layers.

in Table 1 for approximately comparable nano-crystal density but varying injection oxide thickness. The write times are worse than DRAMs (by > 10), but considerably better than flash, and the voltages are low. This tunability of operation - in power and speed - is one of the interesting attributes of these memory structures.

TABLE 1.

Injection Oxide Thickness	Write Condition	Write Threshold Voltage Shift	Refresh Time
1.6 nm	200 ns, 3 V	~0.65 V	>1 wk (RT) ~1 hr (85 C)
2.1 nm	400 ns, 3 V	~0.48 V	>1 w (RT) ~5 hr (85 C)
3.0 nm	1 μs, 3 V	~0.55 V	large (RT) >> 1 hr (85 C)
3.6 nm	5 μs, 4 V	~0.50 V	large (RT) large (85 C)

3 Quantum Kinetic Equation and Time-Constants

We are interested in analyzing the electrical nature of the problem of a quantum-dot coupled to a channel and modulated by a gate A simple electric interpretation of this is a quantum-dot coupled to the gate and the channel modeled by two capacitances (C_1 and C_2) to gate and channel respectively. Due to the absence of scattering, the density matrix equation for this problem can be reduced to a rate equation whose transitions rates can be determined from the transition matrix. A detailed solution of this problem is available in reference [6]. with transition rates determined using coupling constants and occupation statistics. These calculations are quite close to the observations on nano-crystal memories, corroborate the stretching of erase time compared to write, but appear to overestimate the leakage time for single quantum-dot structures. Coupling to the conducting regions and defects should be particularly important to the quantum-dot memories; the calculations do not take this two/three dimensional effect into account.

4 Conclusions

We have outlined some of the features of nano-crystal and quantum-dot memories that can be related to the quantum-confinement and small-dimensions of these structures.

5 References

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