Silicon Nano-Crystal Memory with Tunneling Nitride

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1. Introduction

Nano-crystal memories have been reported [1]-[3] and shown to have good programming and endurance characteristics. This paper presents coulomb blockade effect at room temperature for the first time, of silicon nanocrystal memory with tunneling nitride. Small size, and high density of uniform silicon quantum dots were formed on tunneling nitride. We observed coulomb blockade effect by measuring the saturation drain current after applying successive programming gate voltages. Also, we have obtained better coulomb blockade effect and electrical characteristics in silicon nano-crystal memory with tunneling nitride than that with tunneling oxide. This proves the feasibility of practical silicon nano-crystal memory with tunneling nitride.

2. Device Fabrication

The silicon nano-crystal memory has been fabricated at various dimensions by 0.8µm-standard process. We used deposited 4nm Si₃N₄ as tunneling dielectric. For comparison, devices with 4nm tunneling oxide were also fabricated. The silicon quantum dots were formed through spontaneous decomposition and assembly during LPCVD (Low Pressure Chemical Vapor Deposition) [1]-[4]. Fig.1 shows the SEM(Scanning Electron Microscopy) image of the silicon quantum dots formed on Si₃N₄. Fig.2 shows an AFM(Atomic Force Microscopy) image of the silicon quantum dots. The silicon quantum dots on Si_3N_4 is more uniform than those on SiO2. The quantum dot size is less than 4nm in height and 10nm in diameter. The nano-crystals are covered with 20nm control oxide. The silicon quantum dots which remained after gate photo/etch outside the channel region were removed during the following thermal oxidation step. A poly-silicon film is deposited and etched to form the gate electrode. After the source/drain implantation, a thermal anneal is performed at 850°C for 40min in N2. Fig.3 shows an SEM image of channel region of silicon nano-crystal memory.

3. Results and Discussion

Fig.4 shows the memory operation characteristics. This figure shows hysterisis characteristics of drain current by sweeping the gate voltage back and forth. The threshold voltage shift of ~0.45V for SiO₂ and ~0.60V for Si₃N₄ for maximum gate voltage of only 4.5V was obtained. Fig.5 shows the tunneling dielectrics dependence of write time. After setting the gate voltage abruptly to 5V, the change of drain current for silicon nano-crystal memory with tunneling

nitride is faster and larger than that with tunneling oxide. This may be due to higher tunneling probability resulting from the lower tunneling barrier for nitride. Write time of about 30ms for nitride and 40ms for oxide were observed. respectively. To show the coulomb blockcade effects, in the Fig.6, we measured the saturation drain current after a static gate bias is applied for long time(~1sec) enough to charge electrons fully. The initial curve with no electrons in the dots was obtained by measuring the I-V in a very short time. The important observation in this characteristics is the plateauing of saturation drain current in equidistant steps. For density of 4.8X10¹¹cm⁻² on oxide and 5X10¹¹cm⁻² on nitride, with a control oxide of 20nm, the magnitude of the threshold voltage shift for a single electron per each silicon dot is nearly 0.45V and 0.48V, respectively [1]-[3]. The more obvious plateau in silicon nano-crystal memory with tunneling nitride is indicative of a fair degree of uniformity in silicon quantum dots [1]. Direct tunneling is desired in the charging and discharging of the structure to prevent hotcarrier degradation and allows for the superior endurance characteristics of the silicon nano-crystal memory. Fig.7 shows that the threshold voltage window hardly collapses after 10⁵ cycles.

3. Conclusion

Coulomb blockade effect was observed at room temperature in silicon nano-crystal memory with tunneling nitride. Silicon nano-crystal memory with tunneling nitride showed faster write time and larger threshold voltage shift than those with tunneling oxide. The threshold voltage window in the silicon nano-crystal memories is scarcely degraded after 10⁵ write/erase cycles.

References

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Fig.1 Top-view SEM image of silicon quantum dots on deposited Si_3N_4 .



Fig.2 AFM image of the silicon quantum dots. The dots on Si_3N_4 is more uniform than those on SiO_2 . (a) SiO_2 (b) Si_3N_4 .







Fig.4 Hysterisis characteristics of drain current as a function of gate voltage. (a) tunneling oxide (b) tunneling nitride.



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(b) Fig.6 The saturation drain current vs. static gate bias applied for long time(~1sec) enough to write. The dotted lines represent the I-V curve with zero, one, and two electrons per quantum dots, respectively. (a) tunneling oxide (b) tunneling nitride.



Fig.7 Endurance characteristics of silicon nanocryatal memory with tunneling nitride for \pm 5V pulsing for writing (50ms) and erasing (50ms).