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Characteristics of Narrow Channel MOSFET Memory Based on Silicon Nanocrystals

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MOSFET memory with silicon-nanocrystals-based floating gate on very narrow channel has been fabricated. Large threshold voltage shifts are obtained by applying small electric field to the tunneling oxide for write/erase operation. At room temperature a long retention time is achieved. It is found that the threshold voltage shift is obviously dependent on a channel width, and independent on a channel length. Moreover, the effect of interface traps and defects on charge storage behaviors is discussed.

Introduction

MOSFET memories based silicon nanocrystals or quantum dots operating at room temperature have been investigated extensively and developed rapidly[1-6], due to the promising applications in future VLSI. In this kind of memory structures, direct-tunneling carriers into and off nanocrystals based floating gate shift the device threshold. For the application, in a sense, a large threshold voltage shift under small operating voltage and a long charge retention time at room temperature are the most important. The performance is strongly tied to the devices parameters such as channel dimension, nanocrystal size, and interface traps and defects, etc.[6,7]. In this paper, the characteristics of narrow channel MOSFET memory devices based on silicon nanocrystals having various channel dimensions are investigated.

Experimental

Schematic of the narrow channel MOSFET memory device having silicon-nanocrystals-based floating gate is shown in Fig.1. The source-drain channel is first fabricated on silicon-on-insulator(SOI) substrate using the improved anisotropic etching and selective oxidation method[8] Fig.2 shows SEM image of an as- fabricated narrow channel. Next, silicon nanocrystals are self-assembled at 580°C using 20% diluted SiH_4 gas source on a ~3nm-thick thermally grown tunneling oxide in a low-pressure chemical vapor deposition (LP-CVD) system. Subsequently, an *in-situ* deposition of the gate silicon dioxide layer is deposited. Nanocrystals are evaluated basing on the SEM observation(Fig.3), the average size is ~8nm and the density is $2\text{-}4\times10^{11}cm^{-2}$. Before exposing to air, the sample was sintered at a higher temperature to improve the quality of nanocrystals as well as of the deposited SiO_2. The fabrication process for the gate, source and drain regions is the same as conventional MOS process.

Results and Discussions

MOSFET memory devices based on silicon nanocrystals with various channel parameters are measured, having channel widths of 50 and 100nm and lengths from 0.1 to 1μm. Typical drain current-gate voltage characteristics in these devices after applying a positive/negative voltage for write/erase operation are shown in Fig. 4. Large threshold voltage shift is achieved, which is attributed to the effective screen by silicon-nanocrystals-based floating gate. The write/erase operation can be realized effectively by applying only small electric field of ~2 MV/cm to the tunneling oxide. The devices have an ideal I_d-V_g curve with reasonable on-currents (~μA) and low off-currents (~pA). A striking feature is that the threshold voltage shift ΔV_{th} is obviously dependent on a channel width, and almost independent on a channel length. In the present devices, an average ΔV_{th} is 0.83V for the width of 100nm, and 1.83V for the width of 50nm. In addition, single-electron discharging of the nanocrystal is observed in the narrower channel devices. As an important advantage (Fig.5a), the present narrow channel with a triangle-cross-section is expected to be completely screened by silicon nanocrystals based floating gate. In previous reported devices, however, the channel is only partially screened by the floating gate (Fig.5b), owing mainly to control gate has a capacitance coupling to the channel[4].

Fig.6 shows the retention time characteristics of a device (W=0.1μm and L=0.1μm). Good retention is observed. Owing to the high Coulomb charge energy in nanocrystals, the injected charges are partially rejected back to the substrate in a few seconds after the write/erase operation. In our previous work[6], it has been demonstrated that retention time can be improved by introducing a certain number of deep trapping centers in nanocrystals and decreasing the interface states at SiO_2/Si-substrate. Fig.7 gives the energy band diagram held at a flat-band point in retention mode after injecting electrons. It is suggested that the injected electrons are mainly stored at the deep traps of nanocrystals instead of the conduction band in long-term retention mode. Comparing to MONOS memory structure[9], moreover, the present MOSFET memory structure is more efficient for charge injection and rejection. Here, a charge directly tunnels first into the extensive state of a nanocrystal and then falls to a trap, and stored charge can be extracted directly or recombined indirectly by an opposite pulse voltage.

Conclusions

We have demonstrated that the narrow channel MOSEFT memory device with silicon-nanocrystal-based floating gate has large threshold voltage shifts under small electric field operation, and good retention characteristics. The primary experimental result indicates that narrower channel width has a larger threshold voltage shift. The fabrication and operation of this kinds of devices is compatible with Si MOS technology, promising for the application to VLSI.

References

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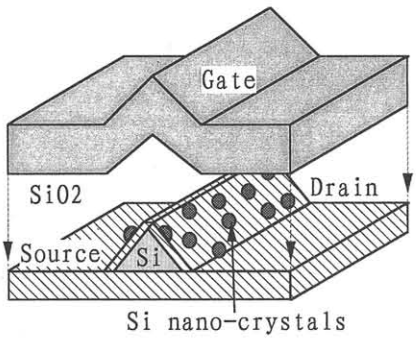

Fig.1 Schematic of the MOSFET memory based on silicon nanocrystal floating gate.

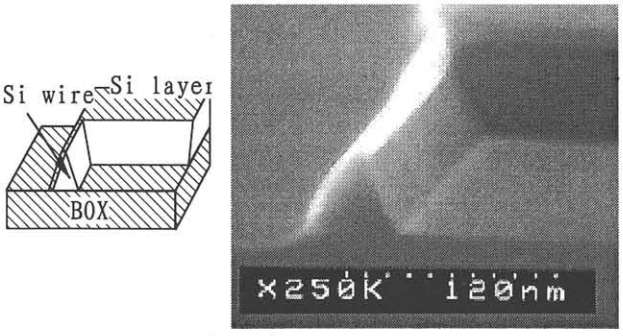

Fig.2 SEM image of cross section of an as-fabricated silicon narrow channel.

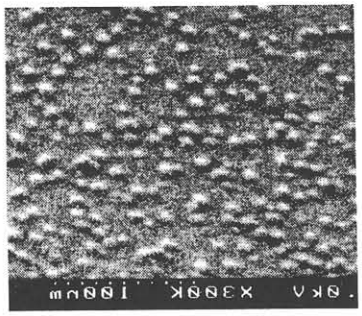

Fig. 3 SEM image of self-assembled silicon nanocrystals on SiO_2.

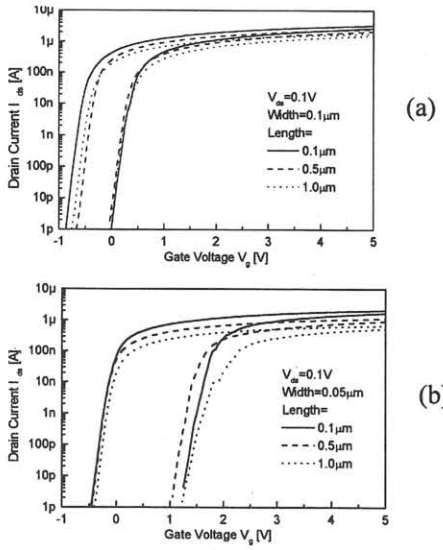

Fig.4 Drain current-gate voltage hysteresis characteristics in the devices with channel widths: (a) 100nm, and (b) 50nm.

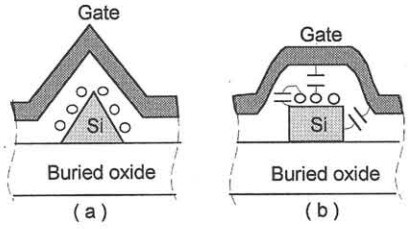

Fig.5. Schematic cross section of the channel showing the capacitive coupling between various elements. (a) This work. (b) Conventional.

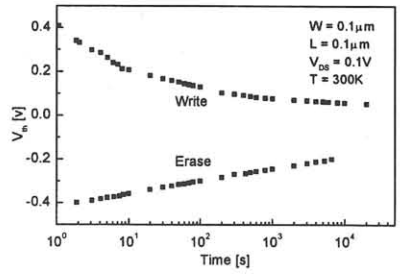

Fig.6 Retention time characteristics of the device in Fig.4(a).

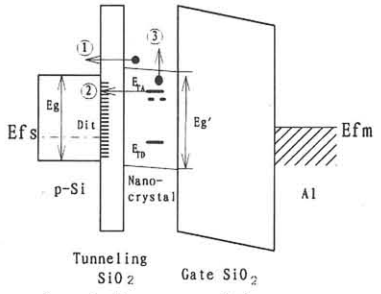

Fig.7 Energy band diagram of the nanocrystal memory structure and electron tunneling processes in the retention mode at flat-band point after injecting electrons.