Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 174-175

Single Electron Charging to a Si Quantum Dot Floating Gate in MOS Structures

A. KOHNO, H. MURAKAMI, M. IKEDA, H. NISHIYAMA, S. MIYAZAKI and M. HIROSE

Department of Electrical Engineering, Hiroshima University, Higashi-Hiroshima 739-8527, Japan
Phone: +81-824-24-7648, Fax: +81-824-22-7038, E-mail: akohno@ipc.hiroshima-u.ac.jp

The transient current of a Si quantum dot floating gate MOS structure with tunnel gate oxides has been measured to reveal the charged state of the dot. It is demonstrated that approximately one electron per dot is stably stored around zero gate bias at room temperature. The memory retention time exceeding 10^3s has been confirmed for a 3.5nm-thick first gate oxide.

1. Introduction

MOS devices with nanometer silicon dots as a floating gate have been fabricated, and their memory operations associated with electron charging to the dots have been demonstrated at room temperature[1-3]. A unique hysteresis in capacitance-voltage (C-V) characteristics of the MOS structures has been interpreted in terms of electron charging to the Si quantum dot floating gate[3]. A key question is how many electrons can be stably stored in one quantum dot under the memory operation. In order to answer to this question charged states of a Si quantum dot (QD) floating gate in the MOS structure have been studied by analyzing the steady state and transient current-voltage (I-V) and C-V characteristics.

2. Experimental

Single-crystalline Si quantum dots were self-assembled on 3.5nm-thick SiO_2 by LPCVD of pure SiH_4 at 580°C[4]. After the first-layer Si dot array formation a ~1nm-thick oxide layer was grown and the second dot array was deposited under the same conditions. The total dot density was ~5×10^{11} cm^{-2} without any significant change in the dot size distribution as measured by AFM. The average dot height and diameter were 5 and 10nm, respectively. The surface of the second Si dot layer was covered by ~1nm-thick oxide. Subsequently, a 3.3nm-thick amorphous Si layer was grown over the Si quantum dots by LPCVD at 440°C and fully oxidized in dry O_2 at 1000°C to fabricate a 7.5nm-thick control oxide. No significant change in the surface morphology was observed in this oxide layer fabrication. Finally, 300nm-thick n^+ poly-Si gates were fabricated. The cross sectional view of a Si QD floating gate MOS capacitor is illustrated in the inset of Fig. 1.

3. Results and Discussion

The measured C-V characteristics of a Si QD floating gate MOS capacitor are shown in Fig. 1. When the gate bias was swept over the range between -4V and +6V, the C-V curve showed the unique hysteresis which arises from electron charging to the dots through the 3.5nm-thick oxide. The steady state C-V curve after electron charging at 6V or after discharging at -4V was determined from the transient capacitance as described in a previous paper [3]. The charged and discharged states are maintained longer than 10^3s at gate voltages between -0.7V and +0.7V (Fig. 1) and write/erase cycles can be repeated, indicating that electrons are stably stored in the Si dots. By analyzing the flat-band voltage shift it is shown that about 1.2 electron per dot is existing as the floating gate charge. Gate voltages higher than +0.7V the steady state C-V curve after charging is identical to that after discharging.

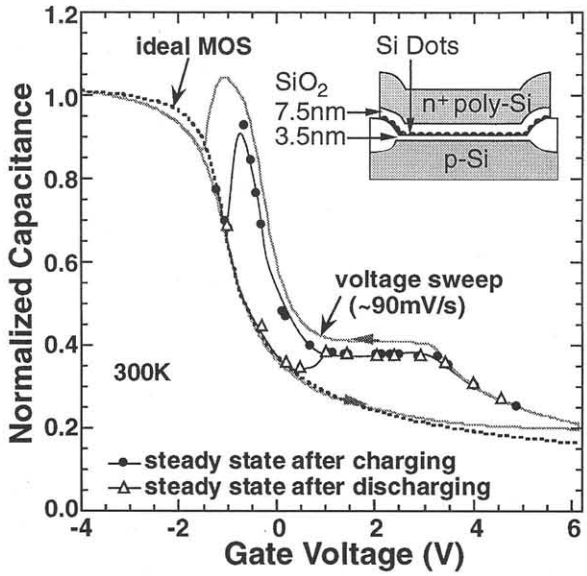

Fig.1 C-V characteristics of a Si quantum dot floating gate MOS capacitor with a gate area of $2.5\times10^{-3}cm^2$. The measurement frequency was 100kHz. The steady state C-V curve was obtained from the transient response under constant bias.

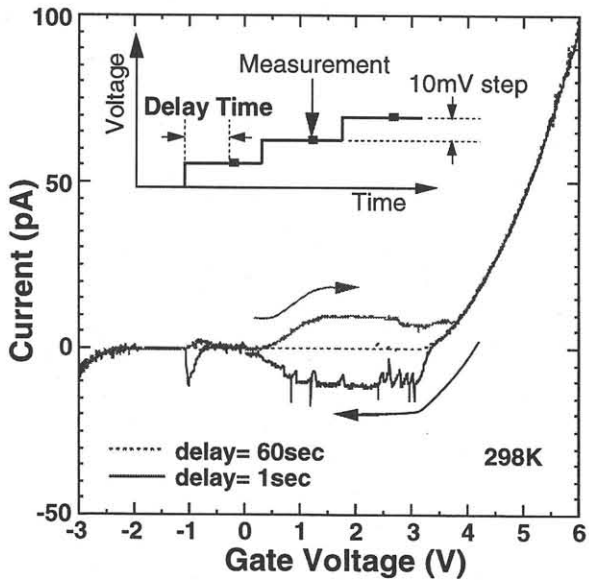

Fig. 2 Current-voltage characteristics of a Si quantum dot floating gate MOS capacitor. The hysteresis due to charging or discharging current is diminished by increasing the delay time after applying stepwise gate voltage.

This is because the tunnel injection current from the substrate to the dots balances the dots-to-substrate or the dots-to-gate emission current at a given gate voltage, and the number of stored electrons per dot determines the capacitance value. On the other hand, at gate voltages lower than -0.7V, electrons in the Si dots are completely released and the device stays in the discharged state or the memory charge is erased.

In order to reveal the transient feature of electron charging or discharging at QDs, I-V characteristics were measured with different delay time after applying stepwise gate bias (Fig. 2). For a delay time of 1s at each voltage step, the I-V curve exhibits the hysteresis, while it is diminished for a delay time of 60s. The origin of the hysteresis is the electron charging to QDs for ramp-up bias or the discharging for ramp-down. Note that around zero bias electrons still remain in QDs as observed by the C-V hysteresis in Fig. 1. The negative current peak around -1 V indicates complete discharging of remaining electrons in the dots. To evaluate the total charge stably stored in QDs around 0 bias, the external gate bias was kept at 0V after writing operation and switched to -1.2V (erased state), and the discharge current was measured as shown in Fig. 3. The non-exponential current decay might be due to the coulombic interaction among electrons stored in the quantum dots. By integrating the transient current, the total dot charge Q_{dot} is obtained to be 2.6×10^{-10} C, which corresponds to the number of retained electron per dot being ~1.3. This is consistent with the value estimated from the flat-band voltage shift of the C-V curve when the charging energy of quantum dot is taken into account.

A distinct increase in the capacitance is also observed when 532nm light is irradiated to an MOS structure at 0V as shown in Fig. 4(a), indicating that electron charging to the dots is caused by tunneling of photoexcited electrons from the Si substrate. As shown in Fig. 4(b), the transient photocurrent at laser ON or OFF is integrated and Q1-Q2 yields about 0.9 electron/dot, being consistent with the result of Fig. 3.

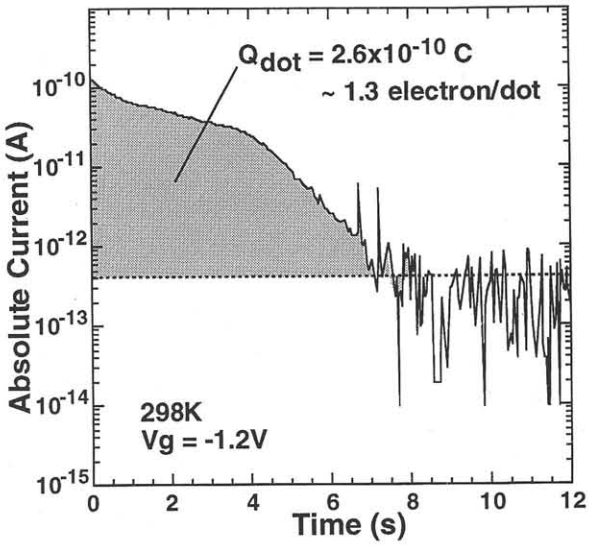

Fig. 3 Temporal change in discharge current from the charged Si dots. The bias was settled from 0 to -1.2V at time 0. The number of electrons retained in one dot is evaluated to be ~1.3.

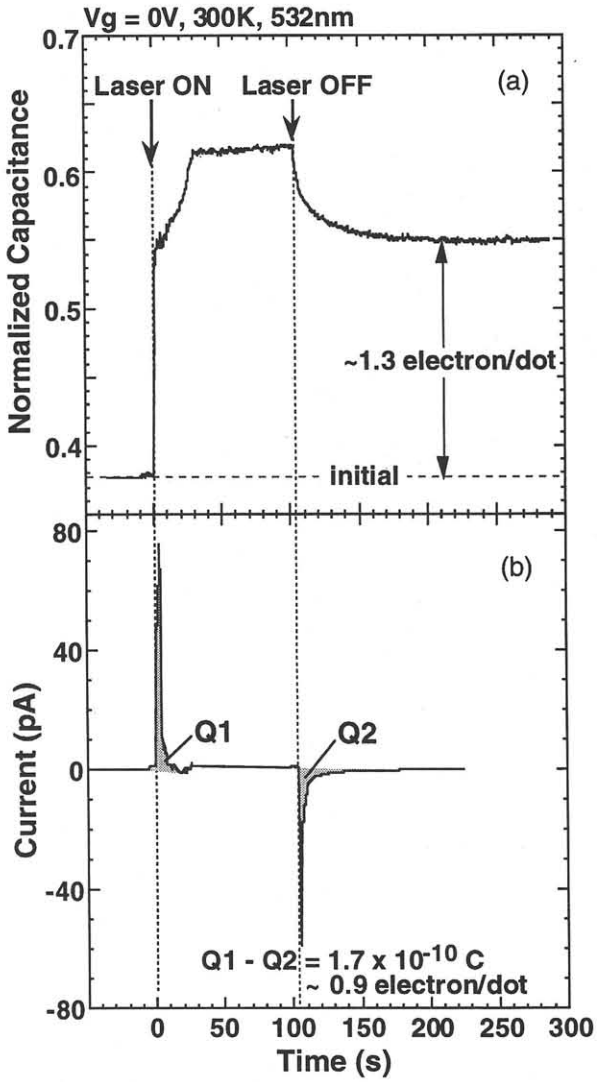

Fig. 4 Transient capacitance (a) and current (b) when the laser irradiation to a Si quantum dot floating gate MOS structure is turned on and off.

4. Conclusions

The electron charging and discharging characteristics of Si quantum dot floating gate MOS capacitors have been quantitatively investigated. The bistability of the charging states for the quantum dots is confirmed around zero bias. The number of retained electron per dot around 0V was evaluated to be about unity from the analysis of the transient current characteristics.

Acknowledgments

This work has been supported by the Core Research for Evolutional Science and Technology (CREST) of Japan Science and Technology Corporation (JST).

References

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