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# A Si Memory Device Composed of a 1D-Wire MOSFET Switch and a Single-Electron-Transistor Detector

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## 1. Introduction

Single-electron devices (SEDs) are promising for future extremely-large-scale integration because of their ultralow-power consumption and highly functional features. In practical applications, especially for interfaces with the real world, they will likely be used in combination with MOSFETs.[1] In this sense, using Si as a base material for SEDs is advantageous with respect to making full use of state-of-the-art MOS technology as well as compatibility with the MOS process.

This paper introduces a novel memory device composed of a single-electron transistor (SET) and a one-dimensional (1D)-wire MOSFET as a first step toward the combined usage of SEDs and MOSFETs. It is shown that the PADOX technique,[2] which we use for self-aligned formation of a SET island and tunnel barriers, is compatible with the fabrication of MOSFETs. It is also clarified that a narrow-channel 1D MOSFET, which is beneficial for size reduction but has been of little practical use because of its low drivability, can be used successfully in SED-based devices, which can operate with a few electrons.

## 2. Device structure and fabrication process

A SEM image of the memory device and its equivalent circuit are shown in Fig. 1. A SET, a memory island, and a 1D-MOSFET channel are formed in a Si-on-insulator layer (30-nm-thick p-type Si layer with a boron concentration of $10^{15}$ cm$^{-3}$) in such a way that the island of the SET and the memory island are coupled capacitively. The SET is used to sense the small number of electrons stored in the memory island. The memory island is connected via a 1D MOSFET to an electron reservoir (side electrode). By using the MOSFET to control electron transport between the memory island and the side electrode, high write/erase speed can be achieved without sacrificing storage time. This is in contrast to flash-memory-type single-electron memories,[3] whose operating speed is limited because of the need for a low tunneling rate between the memory island and channel to assure a sufficient storage time.

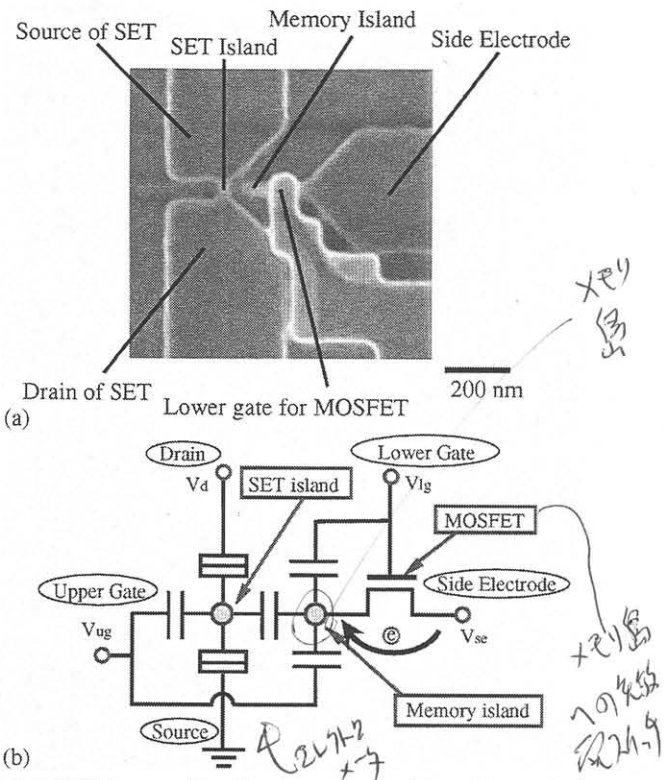


Fig. 1. A SEM image of the Si memory device (a), and its equivalent circuit (b). The initial dimensions of the wire region of the SET were 100 nm long and 40 nm wide, the same as those of the memory island. The gate length of the MOSFET was 50 nm.

After the Si layer was patterned as shown in Fig. 1(a), the 40-nm-wide 1D Si wire sandwiched between the wider Si layers was automatically converted into a SET island with tunnel barriers at its ends by means of PADOX.[2] Next, a poly-Si electrode was formed so as to cover a part of the other 1D-wire region located near the SET island. This electrode, hereafter referred to as the lower gate, acts as the gate of the 1D MOSFET that separates the memory island and the side electrode. Following the gate electrode formation, a $SiO_2$ interlayer and a poly-Si gate electrode (not shown in Fig. 1(a)) were formed successively. The purpose of this upper gate, which covers almost all of the region shown in Fig. 1(a), is to make electrons accumulate in the Si layer under the gate, as well as to control the electrostatic potential of the SET island. This dual-gate MOS configuration is useful for avoiding a complicated process for shallow-junction formation.[4]

In addition to the memory device, 1D-wire MOSFETs were also fabricated on a different wafer in order to investigate their fundamental characteristics. The wire width, i.e., channel width, of these MOSFETs was initially 30 nm, and was reduced to about 20 nm after 8-nm-thick gate-oxide formation.

## 3. Results and discussion

Figure 2 shows subthreshold characteristics of a 1D MOSFET with an 80-nm-long gate. An extremely steep subthreshold swing of 64 mV/dec is obtained at room temperature, which guarantees low-voltage operation. This feature is attributed to the fact that the 1D channel is almost surrounded by the gate electrode.[5] Figure 3 shows the $I_d$-$V_d$ characteristics of the device. As seen from the figure, the conductance is remarkably high irrespective of the channel width of only 20 nm. The subthreshold swing of another 1D MOSFET with a 50-nm long gate degraded to 78 mV/dec, though the conductance increased slightly. Thinner gate oxide, say a few nanometers thick, would improve the performance of 1D MOSFETs with gate lengths less than 50 nm.

Memory operation with a small number of electrons was achieved at 40 K. Figure 4 shows how the device state evolves as the lower gate voltage ($V_{lg}$) is scanned in the positive direction and then in the reverse direction. The side-electrode voltage ($V_{se}$), initially 0 V, was set at -1 V immediately before the start of the $V_{lg}$ scan. The rapid fall of the SET current around $V_{lg}$ = -2.3V, where the MOSFET turns on, corresponds to the "write" action. The written information is held while $V_{lg}$ is scanned back because the MOSFET is off. The number of

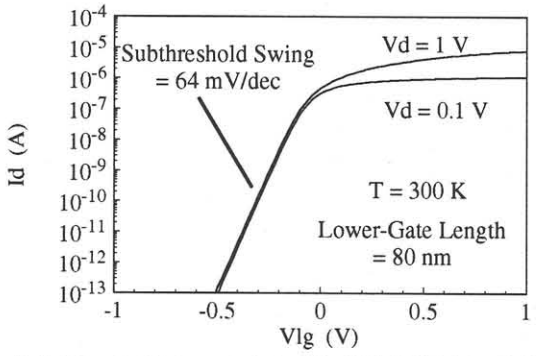


Fig. 2. Subthreshold characteristics of a 1D MOSFET at drain voltages ($V_d$) of 0.1 and 1 V.

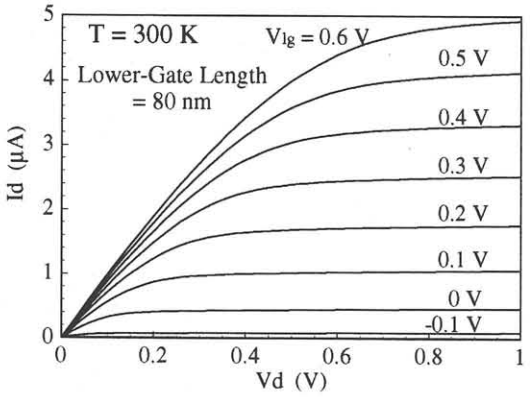


Fig. 3. $I_d$-$V_d$ characteristics of the 1D MOSFET shown in Fig. 2 at verious gate voltages ($V_g$).

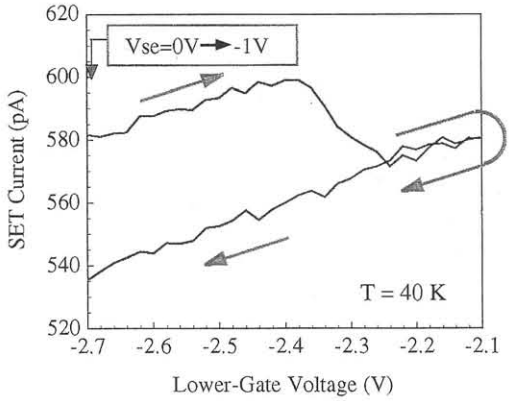


Fig. 4. Hysteresis characteristic of the SET current representing the "write" and "storage" of the Si memory device. The lower-gate voltage was scanned at a rate of 46 mV/s. The slant in the SET current versus $V_{lg}$ is due to capacitive coupling between the SET island and lower gate.

electrons in the memory island for a "write" voltage of -1 V is estimated to be about 100 since the capacitance of the memory island estimated[6] from its structural size is about 15±7 aF. Therefore, in the present memory device, the information "1" can be represented by as few as 100 electrons, and this "1" state is successfully detected by the SET.

Next, we did measurements to check how small a current flowing through the MOSFET can be sensed by the SET. Figure 5 shows the time dependence of the SET current for different $V_{lg}$. The current measurement started just after $V_{se}$ was changed from 0 to -1 V. The MOSFET current estimated from the slope of the initial part of the curves is shown in Fig. 6. As seen

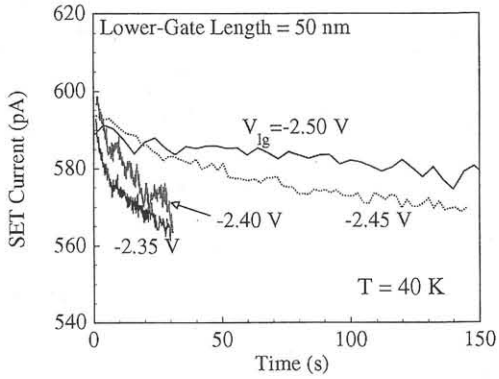


Fig. 5. Time dependence of the SET current for different $V_{lg}$. Measurement started when $V_{se}$ was changed from 0 to -1 V. The change in the SET current reflects the change in the number of electrons in the memory islands.

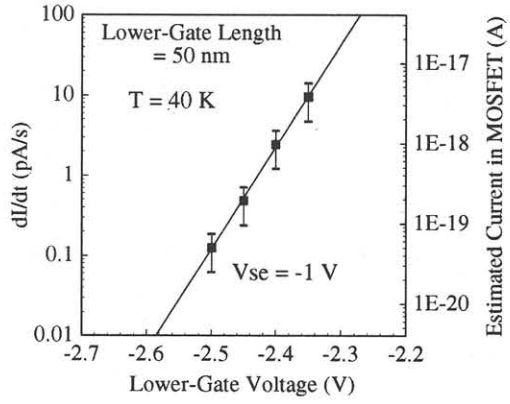


Fig. 6. The subthreshold current flowing through the MOSFET as a function of $V_{lg}$ when $V_{se}$ = -1 V. The current is estimated from the data in Fig. 5. The slope is not steep because the 40-nm-thick gate oxide is formed by PADOX. It could be sharpened by reducing the gate oxide thickness to several nanometers.

from the figure, the SET can sense even a current of the order of $1 \times 10^{-20}$ A.

## 4. Conclusion

A SET and a 1D MOSFET were successfully merged into a memory device using PADOX. The device features a high operating speed and an extremely small number of electrons for representing a bit. It was shown that the 1D MOSFET has a high conductance and a steep subthreshold swing, 64 mV/dec at 300 K, very close to the ideal value. High current sensitivity of the SET was also demonstrated.


## Acknowledgment

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