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Si In-Plane Floating-Dot Memory with a Single Electron Transistor

Toshitsugu Sakamoto, Hisao Kawaura, and Toshio Baba

NEC Fundamental Research Laboratories, 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501, Japan
Phone: +81-298-50-1131 Fax: +81-298-56-6139 e-mail: sakamoto@qwave.cl.nec.co.jp

1. Introduction

The advantage of using of single electron transistors (SETs) with high charge sensitivity as the reading component in a non-volatile memory is that only a few electrons are needed to store information, resulting in high integration and low power consumption. The operation of this type of device with a metallic floating dot has been demonstrated [1]. However, the Si floating dot memory has not been clearly demonstrated because of charge traps near the Si/SiO_2 interface. We develop a Si non-volatile memory with an SET, that is fabricated on a SIMOX (separation by implanted oxygen) wafer with a thin doped superficial Si layer. Because the structure can be easily controlled, the SET shows nearly ideal characteristics [2]. We confirm that the memory can operate at 3 K and the operation occurs not in the unintentional traps but in the artificially fabricated floating dot.

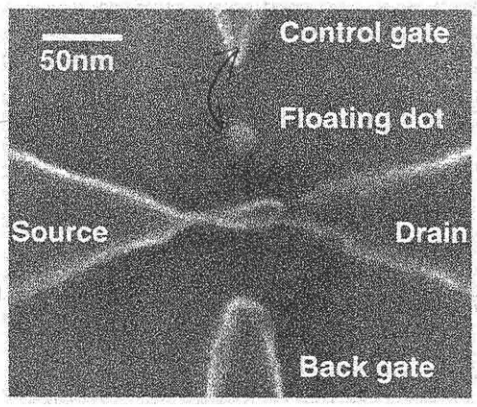

Figure 1: Scanning microscope photograph of an in-plane floating-dot memory.

2. Device structure and fabrication process

The fabrication sequence is as follows. The starting material was a SIMOX wafer with a 20-nm-thick superficial Si layer doped by phosphorus ion implantation. For patterning the structure, we used a calixarene, which is a high-resolution negative resist under electron beam (EB) lithography. The resist shows under-10-nm resolution with a sharp pattern edge [3]. The resist pattern was transferred to the Si film by reactive ion etching with CF_4 gas. The Si surface was then oxidized by 5 nm to remove the superficial layer damaged in the etching process and was passivated by 20 nm chemical-vapor-deposition SiO_2. Figure 1 shows a top view of the fabricated device after the passivation layer was removed. The diameters of the Si SET-island and the floating dot are 30 nm and 15 nm, respectively. The Si surface is depleted and the narrow constriction between the island and the source (or drain) is nearly pinched off. The constriction thus acts as a tunneling barrier.

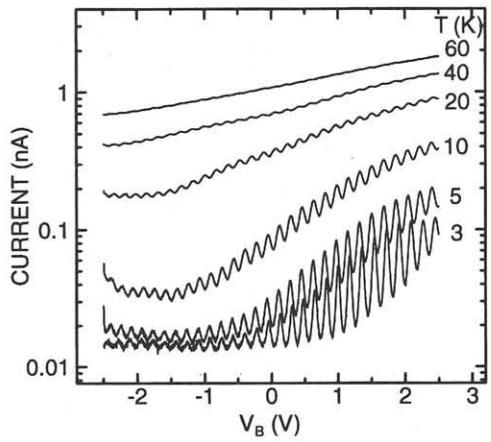

Figure 2: Current versus back gate voltage while control gate is grounded. Temperature is varied from 3 K (bottom curve) to 60 K (upper curve).

3. Device characterization

Electrical characteristics of our device were measured in a ^4He continuous flow cryostat. The device was voltage-biased between the source and drain at $V_{SD} = 1\ mV$ symmetrically. As shown in Fig. 2, the current (I_{set}) oscillated periodically with the back gate voltage V_B and these oscillations could be observed up to 60 K. Based on the period the back gate capacitance C_B can be determined to be 0.88 aF. Similarly, the control gate capacitance C_C can be determined to be 0.47 aF by sweeping the control gate voltage V_C with $V_B = 0\ V$. With the knowledge of C_B and C_C, we could apply voltages to both the control gate and the back gate according to the ratio of $\gamma = -C_C/C_B$, which is about -0.54 for our device. When $V_{C0} > -5\ V$, as shown in Fig. 3, although the floating dot potential was influenced by the gates, the sum induced charge on the SET island was zero and the current was not modulated. As $|V_C|$ was brought to a

SETメモリにおけるバックグラウンドチャージの影響を避けるため、→破壊読出しを行なう。

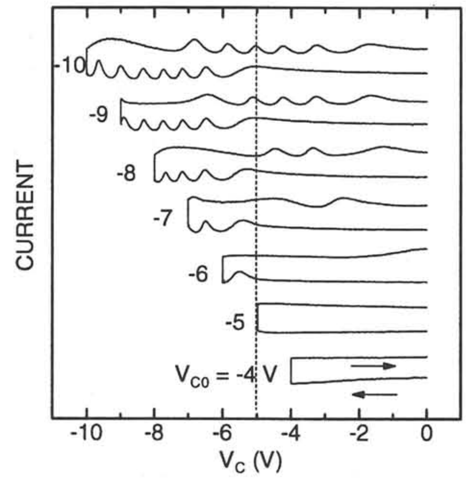

Figure 3: Current of SET versus control gate voltage V_C with a compensation back gate voltage for gradually increased maximum sweep voltage V_{C0}. $V_C = 0 \rightarrow V_{C0} \rightarrow 0\ V$ and $V_B = -0.54 \times V_C$. For clarity, the current in each curve is shifted by 0.1 nA when sweeping V_C back to zero. The onset of the current oscillations for charging in a floating dot is indicated by dotted lines. Temperature and source-drain voltage are 3 K and 5 mV, respectively.

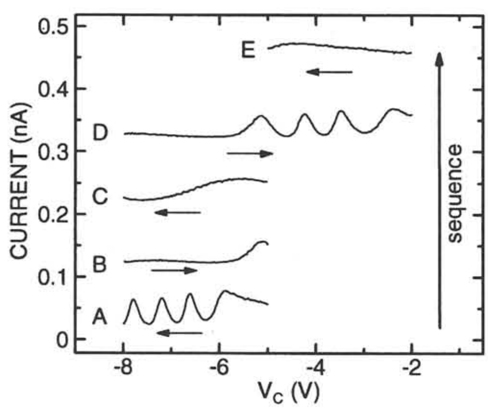

Figure 4: Current when $V_C = -5 \rightarrow -8$ (curve A) $\rightarrow -5$ (B) $\rightarrow -8$ (C) $\rightarrow -2$ (D) $\rightarrow -5\ V$ (E) with $V_B = -0.54 \times V_C$. Each curve is shifted upward by 0.1 nA for clarity.

value greater than the threshold value of $V_C = -5\ V$ (see curves for $V_{C0} \leq -6\ V$), the current started to oscillate, indicating that the potential of the floating dot changed due to a change in the number of excess electrons. Negative V_C lifts the floating dot potential and the barrier is tilted and the electrons can be emitted from the control gate to the floating dot by Fowler-Nordheim (FN) emission. Due to these electrons the potential of the floating dot changes and excess charges are induced on the SET island. Each period corresponds to one induced excess charge e on the SET island. On the way to zero in curves of $V_{C0} \leq -6\ V$ in Fig. 3, the discharge process by a part of excess electrons in the floating dot started at a certain voltage.

To demonstrate the memory function, we charged/discharged the floating dot alternatively by sweeping the control gate voltage to fixed values. The measured current I_{set} for $V_{SD} = 5\ mV$ and $V_C = -5 \leftrightarrow -8$ or $-2\ V$ is depicted in Fig. 4. The charge and discharge processes were seen as current oscillations at curves A and D. Once the floating dot was charged (curve A), a succeeding sweep of V_C of the same direction did not change the dot charge, and the current did not show any oscillation (see curve C in Fig. 4). When $V_C > -5\ V$, the discharge process occurred (curve D). This shows the memory function.

We checked the leakage of the stored electrons by the current I_{set} while V_C was set to be $0\ V$ just after the floating dot was charged by $V_C = -8\ V$. The current started to change after 40 sec due to the discharging. This shows the retention time is short. We also checked the effect of the charging/discharging in unintentional traps around the SET by biasing V_B with $V_C = 0\ V$. When $V_B = 0\ V$ just after biasing at $V_B = \pm 4\ V$, the current I_{set} did not oscillate. Based on the ratio γ, the electrical fields between the SET and the back gate at $V_B = \pm 4\ V$ is roughly equal to the fields between the SET and the control gate at $V_C = \pm 8\ V$. Thus, the value of $V_B = \pm 4\ V$ is high enough to check the charging/discharging in the traps. This supports the idea that the charging/discharging occurs at the floating dot.

4. Summary

We have developed an in-plane Si floating-dot memory fabricated from a doped Si film in a SIMOX wafer by using a high resolution resist. We demonstrate the memory function of this device, which utilizes FN emission and single-electron effects.

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