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High Speed Silicon Single-Electron Random Access Memory with Long Retention Time

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1. Introduction

The operation at 4.2K of a high speed single–electron memory in silicon with two distinct memory states defined by the presence or absence of a small number of electrons has recently been demonstrated [1]. The memory cell is of similar design to that described by Nakazato et. al. [2]. This type of memory differs from single–electron memories described by others [3,4] in that it uses a circuit with two single–electron–tunnelling transistors (SETTs) one to transfer charge and the other to read the charge. The short write time and the absence of the requirement for an erase cycle make this structure attractive for applications where speed is important.

2. Circuit operating principles

The layout of the original memory circuit is shown in figure 1(a). It consists of two SETTs and a memory capacitor. SETT1 controls the number of electrons on the memory node while SETT2 is biased as an electrometer to sense the change of state of the memory. Electrons are written to or removed from the memory node when the voltage across SETT1 exceeds the Coulomb gap voltage of the SETT. Erase is simultaneous with write. The circuit representation of the device is shown in figure (2).

3. Fabrication

The circuit is implemented in a heavily doped ($1x10^{19}cm^{-3}$) n–type silicon–on–insulator SOI wafer using nanowires [5]. High resolution electron–beam lithography and reactive ion etching were used to define the circuit. The original circuit of figure 1(a) was reduced in size by a factor of 30 as shown in figure 1(b). The two circuits are at the same scale and 50nm by 500nm wires define the SETTs in figure 1(b). The compact memory cell was tested for high-speed operation with its reduced capacitances.

4. Circuit performance

Enable pulses were applied to V_{D1} and synchronous write pulses to V_{MC}. The response of the memory to a combined write and enable test cycle was a change of state. The memory only changes state when an enable function, applied to V_{D1}, is coincident with a write pulse, applied to V_{MC}. To demonstrate the speed at which the memory can be operated we applied 5ns write pulses, separated by one minute intervals, to the drain of SETT1. The operation is clearly seen in figure 3 for write pulses as short as 5ns. There is an overshoot on the negative going pulse which recovers to the base level after a few seconds.

The retention time of the memory was investigated under a range of conditions as shown in figure 4 for a test lasting over two hours. Although some drift of level is occasionally seen it is clear that the memory state can be retained for several tens of minutes without significant loss of magnitude.

We have demonstrated that high speed operation of a single–electron memory can be obtained with a long retention time for the memory state without a refresh cycle.

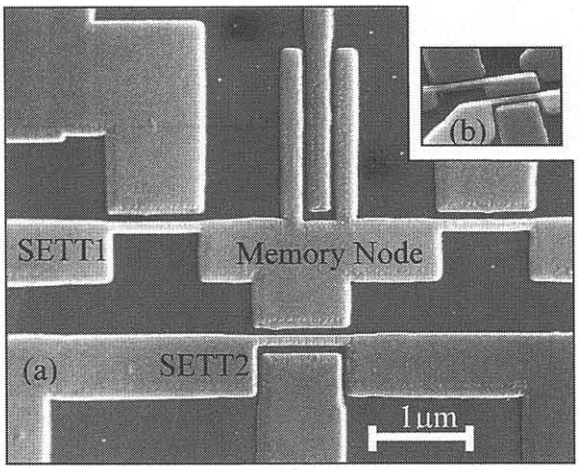

Figure 1(a) Single–electron memory cell with two SETTs and a memory node. (b) Compact version of the single–electron memory with 50nm by 500nm SETTs.

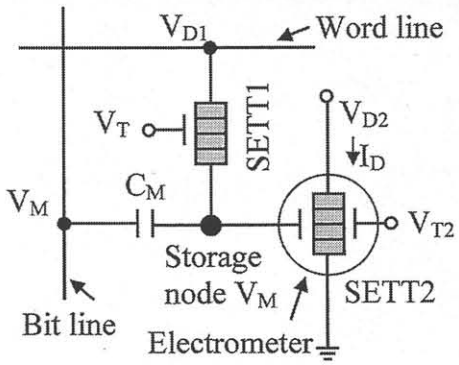

Figure 2 Circuit diagram representing the single–electron memory.

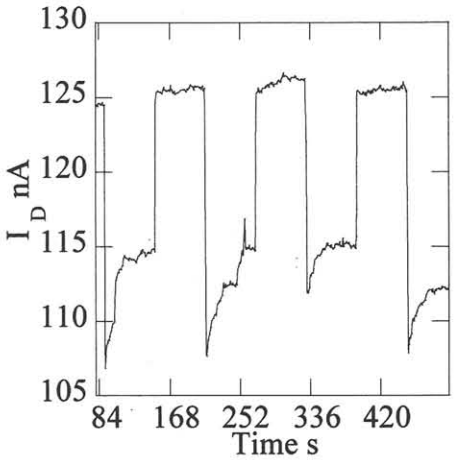

Figure 3 High speed writing to the memory cell with 5ns write pulses.

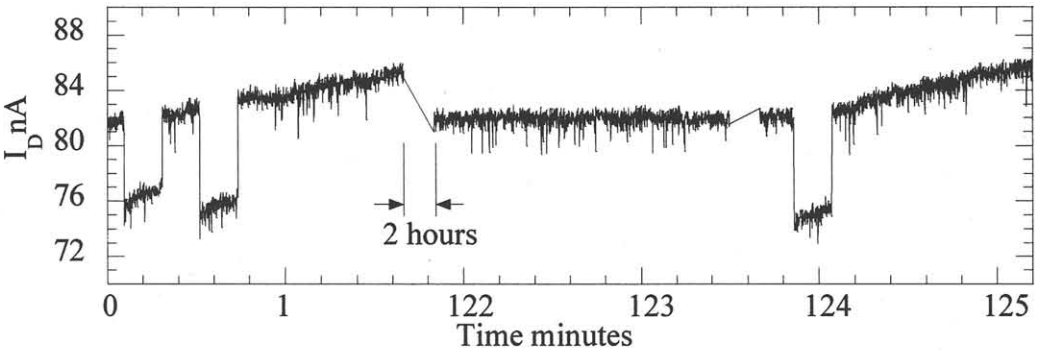

Figure 4 Retention time test after change of memory state.

References

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