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Effects of Electron Tunneling into a Single-Crystalline Si Layer through an Ultrathin Buried Oxide

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1. Introduction

Recently, novel memory devices using ultrasmall Si islands have been studied, where Si nanocrystals or poly-Si grains are often used as memory islands [1,2]. In these devices, it is generally utilized that electrons are injected into the islands through a thin oxide or a grain boundary barrier by direct tunneling from a channel region. However, precise understanding and control of the tunneling process are difficult, because many islands are present in those devices. Furthermore, effects of band bending within the islands, which must be very important for non-metalic islands, have not been studied.

In this work, to clarify the fundamental charging process and the band bending effects, we have fabricated, for the first time, a layered structure of gate electrode / upper oxide (70 nm) / single-crystalline *p*-Si (10 - 50 nm) / lower tunnel oxide (2 nm) / n^+-Si substrate, and studied electron charging effects due to direct tunneling through the buried oxide by *C-V* measurements. Although this structure appears similar to conventional floating gate memories, the following points are completely different; 1) the Si well is single-crystalline and moderately doped and 2) direct tunneling due to the ultrathin oxide is involved instead of Fowler-Nordheim tunneling.

2. Fabrication Procedure

Figure 1 summarizes the fabrication procedure of the SOI structure investigated here. A commercially available bond-and-etchback SOI (BESOI) (001) wafer with the top Si thickness of 330 nm (*p*-type; B: 1×10^{18} cm^{-3}) was bonded to an n^+(As: 5×10^{19} cm^{-3})-Si (111) wafer. Prior to the bonding, a 2 nm-thick SiO_2 layer was prepared on the top of the BESOI wafer (at 700℃ for 10 min in dry O_2), while the native oxide on the (111) wafer was removed in a diluted HF solution. The SiO_2 layer formed on the BESOI surface serves as the buried tunnel oxide layer in the final structure.

Next, the Si substrate and the thick buried SiO_2 layer of the BESOI were back-etched, and an SOI structure having an ultrathin buried SiO_2 layer was obtained. After thinning of the top Si layer by oxidation, uniform top Si layers of 10～50 nm thickness were obtained, on which an about 70 nm-thick SiO_2 layer was purposely left as an upper oxide.

Figure 2 shows a typical TEM image of the cross-section of the fabricated SOI structure. In spite of the annealing at high temperature of 1000℃, abrupt interfaces were found to be kept, and the ultrathin buried SiO_2 layer was also found to remain uniform. It is important that the bonded interface is located between the buried oxide and the n^+ substrate, because charge-trapping effects of the bonded interface will be minimized in *C-V* measurements.

For *C-V* measurements, Au electrode was deposited as a top gate. *C-V* measurements were performed not only under dark condition but also under a halogen lamp irradiation. A high frequency of 100 kHz was used for the ac small signal.

3. Results and Discussion

C-V Characterization

Typical *C-V* curves obtained under dark condition for the SOI structure having top Si layer thickness of 20 nm is shown in **Fig. 3**. Although the top Si layer is *p*-type, the capacitance decreased under negative V_G, being similar to the case for conventional MOS capacitors using *n*-type Si [3].

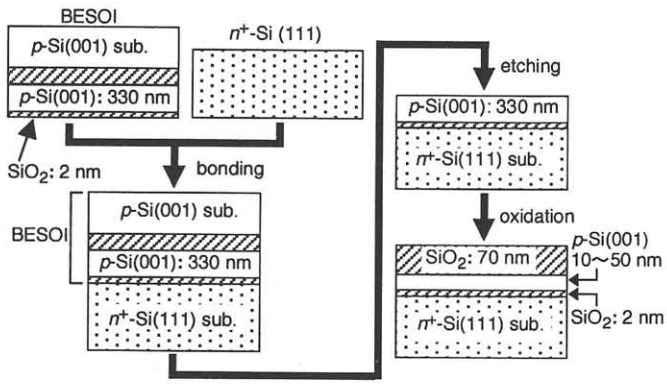

Fig. 1 Fabrication procedure of SOI structure with an ultrathin buried oxide.

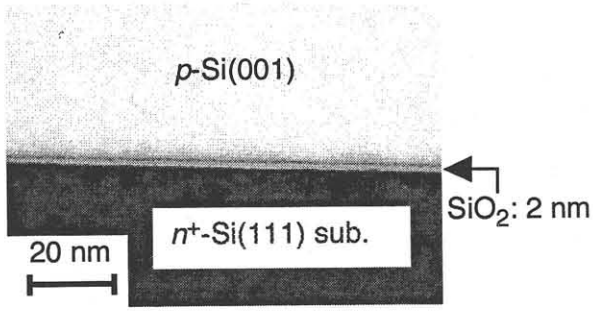

Fig. 2 Typical TEM image of the fabricated SOI structure.

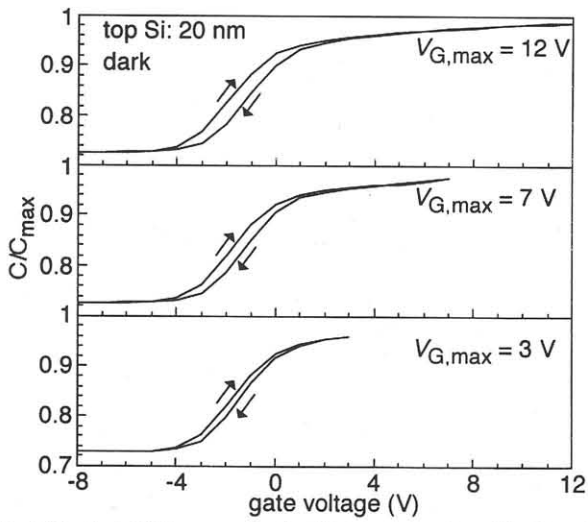

Fig.3 Typical *C-V* curves for the SOI structure (top Si: 20 nm).

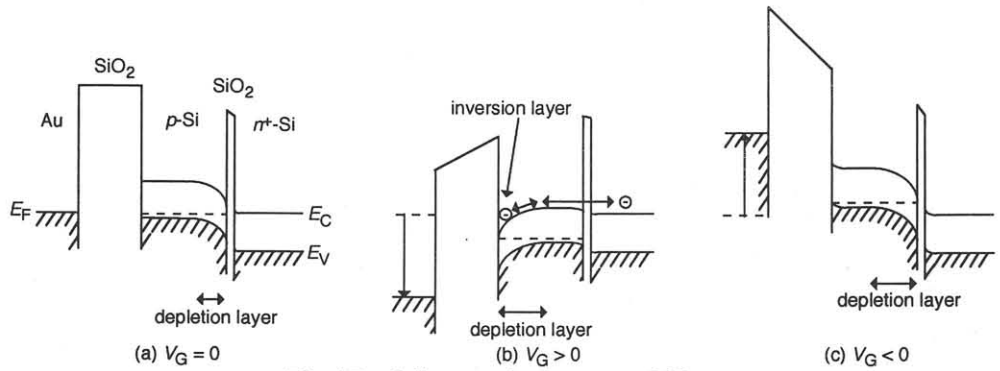

Fig. 4 Band diagrams for the present SOI structure.

However, this result cannot be ascribed to the *n*-Si substrate, because it is heavily doped and the maximum depletion width (5 nm) is too small to explain the measured C_{min}. Therefore, band bending and charging effects in the top Si layer should be most significant and essential.

According to the band diagrams for the present SOI structure shown in **Fig. 4**, the *C-V* curves are qualitatively interpreted as follows.

Under a positive bias, since electrons in the inversion layer at the upper SiO_2/Si interface are supplied from the n^+ substrate through the buried oxide layer by tunneling and almost follow the high-frequency voltage modulation, as shown in **Fig. 4(b)**, the capacitance shows the value of that for the top SiO_2, i.e., $C \sim C_{ox}$, being similar to the low frequency curve for conventional MOS capacitors using *p*-type Si [3]. On the other hand, under negative V_G, due to the depletion layer formation at the interface with the buried oxide shown in **Fig. 4(c)**, the capacitance decreases with the applied negative V_G. In this case, no excess electrons are supplied.

A hysteresis or a shift of the *C-V* curves was also seen in **Fig. 3** for different sweep directions. The amount of the positive shift observed for the downward sweep was found to depend on the maximum value of the applied positive V_G. This suggests that electron tunneling and charging of the top Si layer occurred. These behaviors were commonly observed for the capacitors with different top Si layer thicknesses.

The shift of the *C-V* curve can be interpreted as follows. In a downward sweep, since some of electrons injected at high positive V_G are expected to remain until a small negative V_G, the electronic potential of the floating top Si layer is raised. As shown in **Fig. 5**, this raised potential readily causes the growth of the depletion layer at the interface with the buried oxide, and therefore, the downward *C-V* curve is shifted toward the positive V_G.

Effect of Light Irradiation

In order to confirm the electron charging, *C-V* measurements were performed under a halogen lamp irradiation through thin (20 nm) Au electrode. An example of the results is shown in **Fig. 6**, where the light was irradiated below 0 V in a downward sweep. The capacitance under light irradiation showed the larger value than that under dark condition and approached to the value for the upward sweep. Based on the interpretation for the shift of the *C-V* curve described above, the light irradiation was interpreted to lead to discharging of the top Si layer.

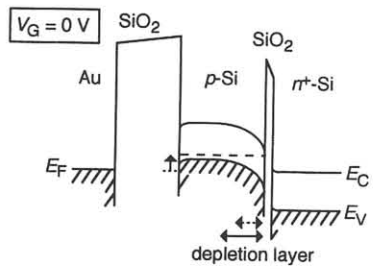

Fig. 5 Band diagram (at $V_G = 0$ V) after electron injection.

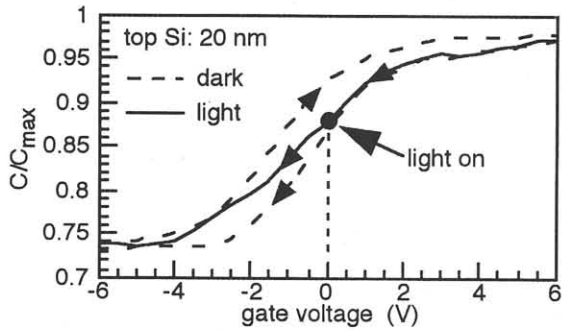

Fig. 6 *C-V* curve obtained under a halogen lamp irradiation.

4. Conclusions

An SOI structure having a thin top Si and an ultrathin (2 nm) buried SiO_2 layers was successfully fabricated by the wafer bonding using an SOI wafer. *C-V* measurements showed that the ultrathin buried SiO_2 layer acts as the tunneling insulator and band bending effects in the top Si layer are responsible for the results. Charging of the top Si layer was also observed as the positive shift in the *C-V* curves and discharging was found to be enhanced by light irradiation.

Acknowledgement

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References

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