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A 128Mb Single-Electron Memory

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1. Introduction

Single-electron memory, which succeeded room-temperature operation only four years ago, has grown steadily to 64-bit integration in ISSCC 1996 [1]. However, the gap between 64-bit memory and state-of-the-art memories, is large. Also the chip-level advantage over conventional memories has yet to be clarified. To fill this gap, we started a project, in which we make a prototype of large scale integrated circuits, to gain insights into the chip level potential of the single-electron memory and also to develop key circuit/device technologies required for integration.

2. One-Transistor Single-Electron Memory

The basic structure uses one-transistor single-electron memory (OSM) scheme. Although the concept of single-electron-transfer had been of interest for limited researchers since the introduction by Likharev [8], single-electron devices worked only at very low temperatures, and, therefore, they were not given much attention in integrated-circuit engineering community. The perception was changed in 1993, when the room-temperature operation was demonstrated and the application of this novel concept was redirected to memory (rather than logic)[2, 3]. Key to these changes was the introduction of OSM scheme, which, up to now, has been the basic platform in the field to prototype and discuss this new technology in the light of applications.

The OSM scheme utilizes one or more dots (or islands) formed in the vicinity of the channel of field-effect transistor, in which trapped charge in the dots modulates the threshold voltage of the FET. Due to this OSM scheme, the main difficulty of the single-electron device, i. e. reading out small charge trapped in dots, has been overcome even at room temperature.

Another favorable feature of the OSM is that it is relatively easy to utilize naturally formed nano-scale dot, which has enabled us to achieve operating device without having to wait until nano-lithography is established. One approach is to use very thin silicon film (about 3-nm-thin) [2, 3], which we call nano-Si film. We found that in nano-Si film both nano-scale dot (or dots) and a narrow channel (or channels) are naturally formed. Based on this device, we demonstrated the first single-electron memory device operating at room temperature [2, 3, 9, 10]. Another approach of OSM scheme is proposed by Tiwari and coworkers [11]. This scheme embeds a number of silicon dots in the gate oxide between the MOSFET-channel and the gate. This structure can be recognized as the parallelized structure of the basic one-dot one-channel structure, and therefore the current drive is improved and expected to have better control than the nano-Si TFT. Yet another approach of OSM is pursued in [12, 13], in which the small dot and a narrow channel are intentionally defined by EB lithography.

We have defined the positioning of this emerging technology to the smallest cell-area technology, which provides minimum bit cost. Although the single-electron memory, which inherently has better scalability over conventional memories, might eventually replace DRAMs and flash memories in the long time frame (this might be 16 giga bit or later), there is difficulty if we try to benefit from this device in shorter time frame. The cell area is determined by the word and data line pitches and difficult to lessen without lithography advances.

3. Verically United Cells

The vertically united cells (VUC) structure is to go beyond the conventional limit by integrating upper and lower cells in $4F^2$ contact-cell area, where 2F is the word and data line pitches [5]. The nano-crystalline silicon-based memory cell previously reported [2, 3] has much simpler structure than conventional memory cells. Here we utilized this degree of freedom to make the memory current direction vertical and unified two-bit cells in a contact area. Note that two cells share many components, such as word line, source line, channel silicon, all of these components are simultaneously fabricated in both cells. Therefore, the increase of process steps to go from a one-storied cell to two-storied cells is only 5 %.

The challenge of VUC array is how to control the upper and lower cells separately, when they share a word line and a global data line. The sharing of the global data line is necessary, because the narrow data-line pitch does not allow placing of separate two lines. In the control scheme, all the operations are word-line based as in [1], however, the upper and lower local data lines are controlled in a time-multiplexed manner to meet the above requirements.

4. Circuit Technologies

The major obstacle against large-scale integration is cell characteristics variations, which include process variations and stochastic electron-count variations inherent in single-electron memories [4]. Stable read/write is accomplished using folded-data-line-based dummy-cell architecture. A dummy cell, which has the same structure as the memory cell, is used. Because the same dummy cell is referenced for both write (with verify sheme as explained later) and read, the memory cell threshold is automatically controlled around the dummy-cell threshold. This dramatically improves the temperature/voltage variation margins. Conventional folded-data-line scheme used in DRAMs, however, generally has considerable area penalty, because the same word line cannot be shared by its spouse data line, therefore, its use in single-electron memory might erode VUC advantage. To overcome this, the proposed scheme is combined with three-dimensional selection arrangement, which allows us to share the same word line between pair data lines. This is because the upper/lower selector cut-off the data-line current drive of the spouse cell, while dummy cell is driving the spouse global data line. Due to this architecture, the area penalty due to the folded data line is negligible.

Another new technique to overcome the variations is bipolar verify scheme. There has been deep concern in single-electron device research community that the reliable operation of such a device might be impossible because of its inherent stochastic electron-count variations, especially when the probability tail cannot be neglected in large scale integration. Although verify scheme itself is well known in flash memory community, we have

found that this technique works very well to overcome the variations [6]. The proposed bipolar verify scheme checks finishing of both write and erase. This is relatively easy in our nano-Si memory, because there is no forward bias problem in our cell which does not have pn junctions. Compact circuit for this bipolar verification is achieved using source follower current amplifier circuit combined with pass-only-high-level circuit.

5. Experiments

Using these techniques, an experimental 128-Mb (8k x 8k x 2) memory is designed and fabricated. Although the memory cell is based on 0.25 μm technology, the cell size is as small as 0.145 μm^2/b, which is close to the effective cell size of the 4-Gb DRAM published at ISSCC97 [7]. A local data line is shared by 64 cells and, therefore, one block, upper and lower local data lines, includes 128 cells. One global data line is shared by 128 blocks. Read, write, and erase are simultaneously done using a word-line as the basic unit, which consists of 8k cells. All the data are transferred serially by the 32 sets of shift registers. The peripheral circuits use 0.4-μm CMOS technology, except the high voltage transistors for write/erase use 1-μm channel length.

6. Remaining Issues and Future Challenges

Although 128-Mb integration has been demonstrated, there remains a long way off to manufacturable memory device. One debatable aspect is whether we should rely on naturally formed structures or not. The above integrated-circuit level experiments have heavily relied on naturally formed dots and narrow channels in nano-Si thin film, therefore, the natural structure has been the weapon to proceed forward in demonstrations. However, this is at the expense of device-characteristics control compared to more artificially structured device. Although the experimental device characteristics in more should-be-controlled devices [12, 13], so far, do not show better control capability than nano-Si TFT device in their experiments, the efforts for better control should be pursued. One interesting possibility is to use self-formed structures. The scattering suppression circuits, such as verify [6], are key to manufacturable device and should be given more studies.

The advantage of the single-electron memory over conventional technologies should also extensibly be researched and discussed. One strong incentive of this research has been the anticipation for better down scaling capability, however, it is yet to be confirmed theoretically and experimentally. The digital-information storage era has just begun, and the need for low-cost low-power memory technologies should increase as time proceeds. It is still yet to be clarified whether the single-electron memory will become the key device in this era. However, the challenges are becoming more and more concrete and waiting to be tackled.

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