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Room Temperature Operating CMOS-like Logic Circuits with Single Electron Tunneling Devices

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1. Introduction

Single electron transistors (SET) are promising candidates for future functional devices because of their operation principle applicable to an atomic scale. Therefore, there have been many studies of constructing logic circuits with SETs [1-3]. One possible way to imitate CMOS logic circuits by substituting SETs for MOSFETs is attractive, because the methodology of CMOS LSI is straightly applicable.

This paper shows the feasibility studies of room temperature operation of CMOS-like SET logic circuits, and the possible way of it is also proposed.

2. Feasibility Study of CMOS-like SET Logic

To use an SET shown in Fig. 1(a) as an nMOS-like logic switch, a "high"/"low" logic-level gate voltage needs to break /maintain Coulomb blockade conditions.

First, assume the simplest case as shown in Fig 1(b): no fractional charge and no back-gate capacitance. If "high" gate voltage breaks the Coulomb blockade, "high" drain voltage breaks the Coulomb blockade regardless of the gate voltage. Thus, the SET can not work as an nMOS-like logic switch in the conventional CMOS-like logic circuits.

Second, considering that the Coulomb blockade region can be adequately offset by a fractional charge without any additional capacitance, shown in Fig. 1(c), the gate voltage can switch the SET, even at the "high" drain voltage. Graphical consideration in Fig. 1(c) point out that the optimum charge, which makes the off-leak current smallest, is $e/6$ that correspond to $e/3C_\Sigma$ of power-supply voltage. Next, suppose that the gate voltage can be offset by the back-gate voltage, but that there is no fractional charge. The drain voltage available in this case needs to be greater than $e/2C_\Sigma$ on the assumption that the back-gate voltage is equal to the "high" level voltage. As long as above qualitative consideration is concerned, it seems that the intentional Coulomb oscillation phase control might be a solution for CMOS-like logic circuits. So we have focused on the on-off ratio of the SETs: the ratio of maximum/minimum current of Coulomb oscillations. The numerically calculated results with master equations are plotted as a function of temperature for three drain voltages in Fig. 2, here the temperature and the drain voltages are normalized by the charging energy and the blockade voltage, respectively. The vertical solid line is defined by the ratio of the room temperature to the charging energy of 1nm-diameter Si sphere self-capacitance. To use SETs as logic switches, we reasonably assume that the on-off ratio greater than 10^3 is needed. The dotted area in Fig. 2 defines a fundamental limit for logic circuit operation. In fact, more strict constrains make the region much smaller. As an example, Fig. 3 shows that finite tunnel junction capacitances make the V_D dependence of Coulomb oscillation phase more complicated, compared to the simple consideration in Fig. 1. The charging energy equal to the operation temperature is also too optimistic for logic operation. Thus we conclude that by merely substituting 1nm Si-SETs for MOSFETs, CMOS-like logic circuits never work properly at room temperature.

3. Clocked Charging/Discharging SET Logic

The SET operation as logic switches requires the power-supply voltage lower than the gate voltage swing. We should compensate the voltage mismatch by amplifying the SET output with other devices. The CMOS buffer/amplifier is suitable for this purpose [4]. Now, we propose the circuits which consist of low-biased SET logic trees and CMOS buffer/amplifier, as shown in Fig. 4. It is important that input/output voltages are equal to the power-supply voltage of CMOS circuits. Since we have already verified CMOS buffer operation in the experiments [5], the functional operation of SET logic tree is a challenging target. As an example, we pick up the four-way XOR circuit as shown in Fig. 5. Note that this circuit is realized by substituting the SETs using the lower power-supply voltage for logic tree MOSFETs [6]. Another important point is that this circuit is not the pass-transistor logic. Thus, it is not necessary to transfer "high" level, but the SETs are only used for discharging.

The hybrid simulator, in which the single electron tunneling simulator and SPICE are hybridized [7], was used for the operation analysis in the circuit in Fig. 5. The functional operation was confirmed as shown in Fig. 6, where total capacitance, equal to the self capacitance of 1nm Si sphere and 293K were assumed.

4. Conclusions

In this paper, we have shown a possible way of CMOS-like logic circuits with SETs by using the clocked charging/discharging SET logic tree. It consists of SET logic trees and CMOS buffers/amplifiers, and the circuit operation has been confirmed by the simulator even at 293K in the condition of the SET with the total capacitance equal to self capacitance of 1nm-diameter Si sphere surrounded by SiO_2.

Acknowledgments

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References

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[6] L. G. Heller *et al.*, *ISSCC Dig. Tech. Papers*, (1984) 16.
[7] This simulator was accomplished in the collaboration with Hitachi Cambridge, Osaka University, and Toyo University as a part of the MITI program on deca-nano integrated circuits supported by NEDO.

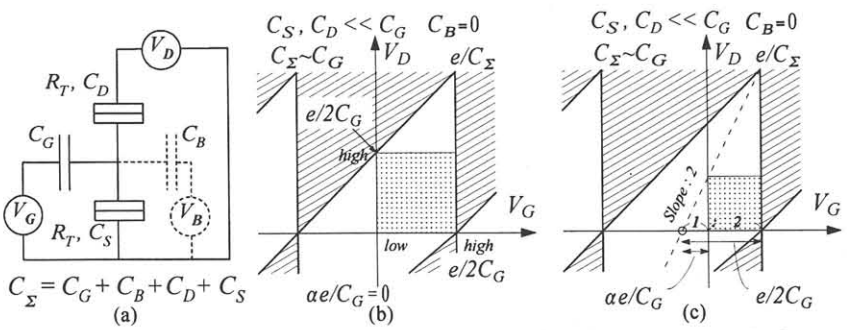

Fig. 1 : (a) A schematic drawing of a single electron transistor (SET). The back-gate is optional. (b) The "low" gate voltage should turn the SET off even at the "high" drain voltage. (c) Assuming that the Coulomb oscillation phase can be adequately offset by the fractional charge, the "low" gate voltage can turn the SET off even at the "high" drain voltage. The optimum charge, $e/6$, makes the off-leak current of the SET smallest. In this case, the drain voltage is equal to $e/3C_\Sigma$. Here broken line is defined by the gate voltage which provides minimum current of Coulomb oscillations at a finite drain voltage. If the background charge is generated by the back-gate voltage equal to the power-supply voltage through the back-gate capacitor, the optimum logic swing should be greater than $e/2C_\Sigma$.

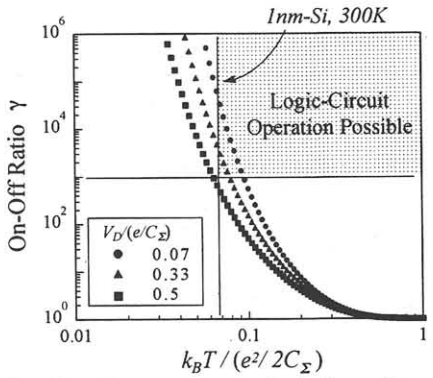

Fig. 2 : Temperature and drain voltage dependence of the on-off ratio of SETs. Temperature and drain voltage are normalized by the charging energy and the blockade voltage, respectively. The vertical solid line is defined by both the self-capacitance of 1nm-diam. Si sphere and room temperature. The dotted area shows the possible operation region of the CMOS-like logic of SETs

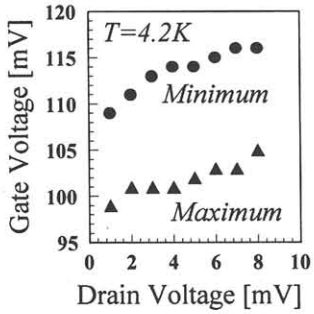

Fig. 3 : The experimental relation between gate voltage and drain voltage which provides minimum or maximum current of Coulomb oscillations in the Si-SET.

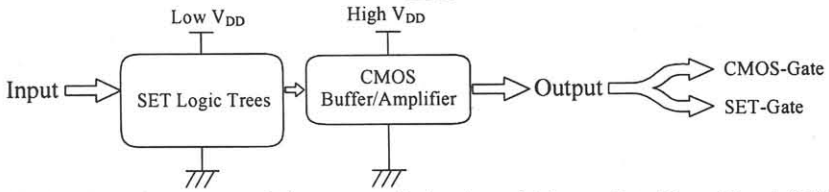

Fig. 4 : A basic concept of the proposed circuits, which consist of low-biased SET logic trees and CMOS buffer/amplifier. Input/output-voltages are equal to the power-supply voltage of CMOS circuits.

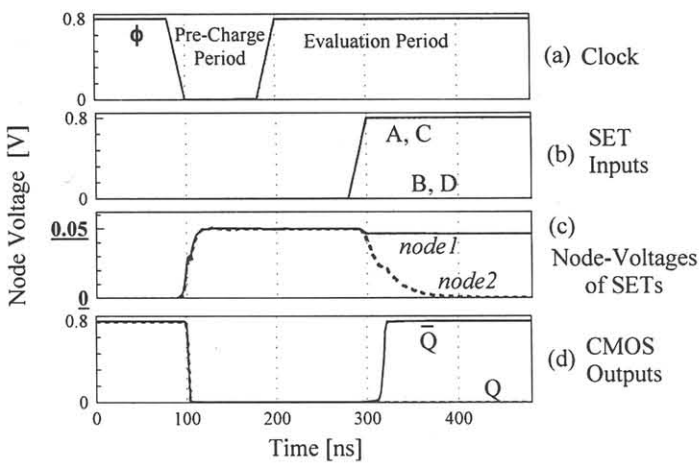

Fig. 6 : The timing chart of the circuit shown in Fig. 5. First, the clock is lowered to "low" level (80-100ns), and the node 1 and 2 are pre-charged. Second, the clock is pulled up to the "high" level (180ns-200ns) and the input-voltages are transferred to the gate of the SETs (280ns-300s). Thus, one of the two nodes is discharged and the other node remains its logic-level. These node-voltages are amplified by CMOS inverters to the power-supply voltage level of CMOS as shown in (d). Here C_G=0.1aF, C_S=C_D=0.06aF, R_T=500kΩ, C_L=10fF, C_F=1fF, C_f=50aF, v_{dd}=50mV, V_{DD}=0.8V, and T=293K. The calculation was performed by the hybrid-simulator [7].

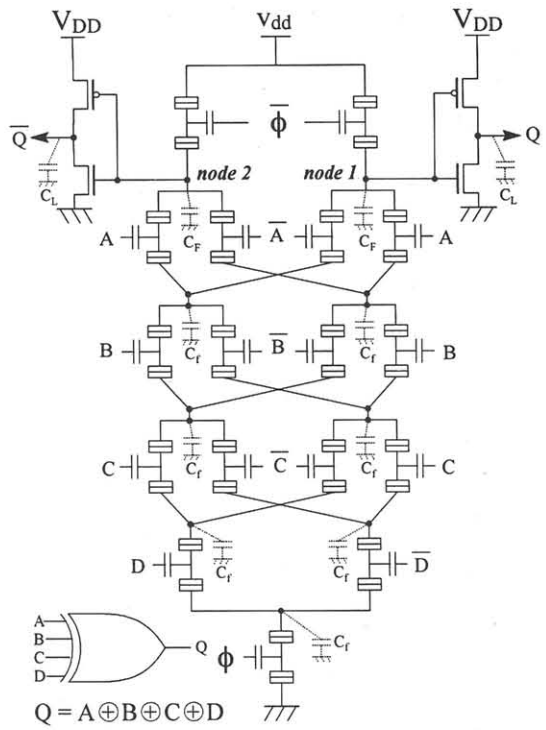

Fig. 5 : Four-way XOR circuit. The SET logic trees are biased by the lower power-supply voltage v_{dd}, while the CMOS amplifiers are biased by the higher power-supply voltage V_{DD}.