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Macro-Modeling of Single Electron Transistors for Efficient Circuit Simulation

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1. Introduction

Recent achievements in the fabrication of single electron circuits such as a memory array [1] are prominent and the era of single electron integrated circuits seems to begin already. In parallel, there have also been a lot of efforts for the development of single electron circuit simulators and a couple of simulators have been opened for the public [2-4]. In these simulators, Monte Carlo methods are used for the probability calculation of all the Coulomb islands in the circuit and a great amount of simulation time is usually needed. For efficient design and simulation of single electron circuits, however, a compact model would be required such as in the case of conventional circuit simulators (SPICE). Recently, it has been found that the current-voltage characteristic of each SET can be independent with those of other SET's when the load capacitor at the interconnection is large enough [5]. In that regime, the compact model could naturally be used.

This paper presents the development of a SPICE macromodel of the SET for efficient simulation of single electron circuits. The macromodel is used for the simulation of complicated circuits such as an inverter and a NOR gate. The macromodel efficiently reproduces Monte Carlo calculation results with a reasonable accuracy.

2. Macro-Modeling

Figure 1 shows the proposed SET equivalent circuit and its macromodel code. Symmetric features of the drain-source current-voltage characteristics are incorporated with two branches consisting of the combinations of resistors, diodes, and voltage sources, which are denoted by R2/D2/V2, and R3/D3/V3, respectively. The directions of D2 and V2 are opposite with those of D3 and V3 to have adequate current flow in both positive and negative drain-source bias. The charging energy, periodically changing as a function of the gate bias, is included in R1, R2 and R3 where the cosine of the gate bias is used. They are expressed as follows;

$$R_1(V_G) = CR1 + CR2\cos(CF1 \cdot V_G)$$
$$R_2(V_G) = R_3(V_G) = \frac{CVp}{CI2 - 2CVp/R_1(V_G)} \quad (1)$$

The parameters, CF1, CVp, CI2, CR1, and CR2 are used to fit the current-voltage characteristics at various gate biases. Figure 2 shows the simulated I-V characteristics of an SET at various gate biases. The solid lines are the Monte-Carlo calculation results and the open symbols are the macromodel calculation results. The SET has the gate capacitance, C_g = 3.2 aF, the junction capacitance, C = 1.6 aF, the tunnel resistance, R_t = 100 MΩ, and the temperature, T = 30 K. With a proper choice of the parameters, CF1 = 60, CVp = 0.02, CI2 = 0.2×10^{-9}, CR1 = 300×10^{6}, and CR2 = 100×10^{6}, the macromodel calculations reproduce the Monte-Carlo calculations reasonably well. Since the current-voltage characteristics of SET's strongly depend on T, the macromodel parameters are the functions of T. The parameter values at various T's are summarized in Table I.

3. Simulation Results of Single Electron Circuits

The macromodel has been applied for the simulation of several single electron circuits. The voltage transfer characteristics of a single electron inverter and a NOR-gate are shown in Fig. 3 (a) and (b). The load capacitance, C_L = 400 aF is used for both circuits and the values of C and C_g are denoted in the figure. The same macromodel parameters are used for all the SET's in the circuits and they have not been adjusted to fit the transfer characteristics. The macromodel results (empty symbols) are in good agreement with the Monte Carlo simulation results (filled symbols) [4-6]. Moreover, it has to be emphasized that orders of less CPU time is need for the macromodel calculations than the Monte-Carlo calculations. The efficiency of the macromodel calculations allows a prompt evaluation of the deigned logic gates.

4. Conclusions

This paper presents SPICE macro-modeling technique for the compact calculation of single electron circuits. The developed macromodel has been used for the simulation of the inverter and the NOR gate and the macromodel calculations match well with the Monte-Carlo calculations even though the orders of magnitude less CPU time is taken in the macromodel.

Acknowledgements

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References

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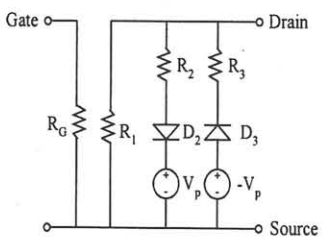
3. SIMON (C. Wasshuber and H. Kosina, "A Single-Electron Device and Circuit simulator", *Superlattices and Microstructures*, **21**, 37 (1997).).
4. KOSEC (KOrea Single Electron Circuit simulator) is developed in the Nanoelectronics Lab. in Korea Univ, Seoul, Korea.
5. Y. S. Yu, H. S. Lee, and S. W. Hwang, "SPICE-type calculation of single-electron circuits", *Ext. Abs. of ICVC 97'*, 549 (1997).

(a)



(b)

```
.option post
.macro SET 1 2 3
.param
+pi=3.1415926535897932846
+CF1=40              ; 2C_G/e
+CI2=0.2e-9
+CR1=300e+6
+CR2=100e+6
+CVp=0.02
V2 5 3 DC CV
V3 7 3 DC '-CV'
RG 2 3 100G
RR1 1 3 R='CR1+CR2*cos(CF1*pi*V(2,3)'
RR2 1 4 R='CVp/(CI2-2*CVp/(CR1+CR2
+*cos(CF1*pi*V(2,3))))'
RR3 1 6 R='CVp/(CI2-2*CVp/(CR1+CR2
+*cos(CF1*pi*V(2,3))))'
D1 4 5 DIODE
D2 7 6 DIODE
.MODEL DIODE D(N=0.01)
.eom
```

Fig. 1 Macro-modeling of an SET (a) the equivalent circuit of an SET (b) the SPICE macro model code.

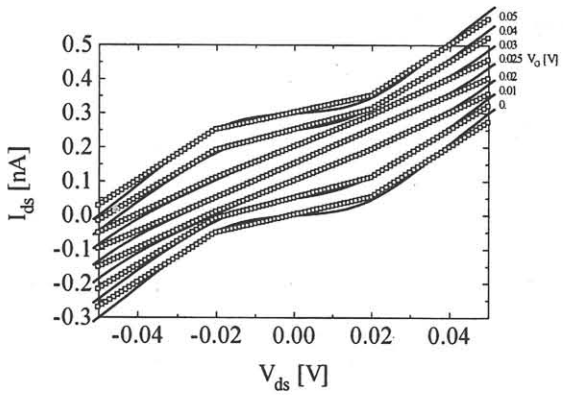
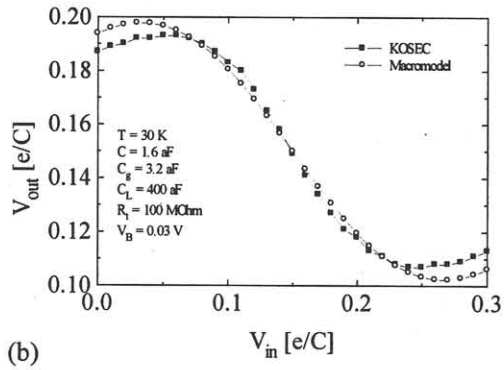


Fig. 2 The current-voltage characteristics of an SET at various gate biases.

Temp. / Para.	10 K	30 K	77 K	100 K	300 K
CI2	0.2 n	0.2 n	0.25 n	0.27 n	0.35n
CR1	1.35 G	300 M	168 M	147.5 M	118 M
CR2	1.15 G	100 M	14 M	4.5 M	0

Table 1 The macromodel parameters at various temperatures. The parameter, CF1 (= 40) is temperature independent.

(a)



(b)

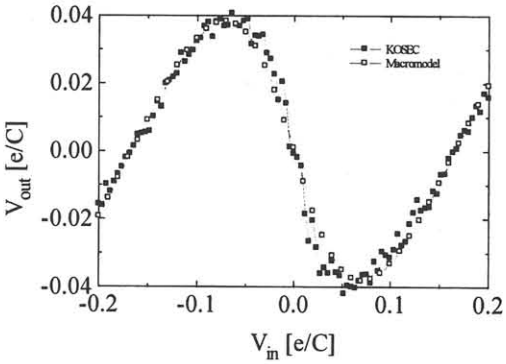


Fig. 3 The voltage transfer characteristics obtained from the SPICE macro-model of (a) the single electron inverter and (b) the single electron NOR-gate.