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Observation of Coulomb Blockade in Resistively Coupled Single Electron Transistor

Yuri Pashkin[1,*], Yasunobu Nakamura, and Jaw-Shen Tsai

NEC Fundamental Research Laboratories, 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501, Japan
tel.: +81-298-50-2602, fax: +81-298-56-6139, E-mail: pashkin@qwave.cl.nec.co.jp
[1] Japan Science and Technology Corporation, 1-8, Honcho 4-chome, Kawaguchi City, Saitama 332-0012 Japan

1. Introduction

Single electron transistor (SET) [1] is one of the simplest and most promising circuits of single-electronics for future applications. It consists of two ultrasmall tunnel junctions connected in series with a gate attached to the island between the junctions. The operation of the transistor is based on the fact that small continuous charge supplied by the gate causes changes in the current-voltage (I-V) characteristic of the device. These changes can be easily observed provided thermal and quantum fluctuations are small.

Depending on the type of the gate, two versions of the SET are possible [2]: one with a capacitive gate coupling (C-SET) and another, with a resistive gate coupling (R-SET) (Fig.1a). Although C-SETs have been realized successfully in a great variety of forms, the implementation of R-SET has been a challenge for experimentalists so far. Although more complicated in fabrication, R-SET has advantages which can make it competitive with C-SET. First, it does not suffer from the background charge fluctuations because a small charge leak is provided through the gate. Second, a high voltage gain ($K_V \gg 1$) is predicted in R-SET due to a specific Coulomb blockade region with sharp edges (Fig.1b). However, recent theoretical analysis [3] has shown that because of the Nyquist noise of the gate resistor, the operation of the R-SET degrades drastically with temperature with no voltage gain possible at $T \geq 0.02e^2/k_B C_\Sigma$, where C_Σ is the total capacitance of the island.

So far, only one attempt in the fabrication of R-SET with 1D array of tunnel junctions as a gate has been reported [4], however, the regime of its operation was far from the theoretical prediction.

Here we report the first implementation of the originally proposed R-SET [2] comprising two small tunnel junctions and resistive gate attached to the island. We measured current-voltage (I-V) and transfer (V-V_g) curves of the transistor and found a fair qualitative agreement with simulations based on the orthodox theory of single electron tunneling.

2. Experiment

The Al/AlO_x/Al tunnel junctions and Cr thin-film resistive gate were fabricated using e-beam lithography and three-angle evaporation. The details of the fabrication procedure are described elsewhere [5].

The transistor is designed such that the Cr gate is connected to the middle of the Al island which is 45 nm x 300 nm. The area of each junction, as concluded from the SEM image of the R-SET, is about 0.001 μm^2. The gate is about 60 μm long and 30 ~ 40 nm wide.

Measurements were performed in a dilution refrigerator at a base temperature of about 50 mK. A high magnetic field (1 T) was used to quench the superconductivity of aluminium. With our set-up (Fig.1a), we could sweep or step bias voltage V_b and gate voltage V_g and measure voltage drop V across both junctions and current I through the first junction.

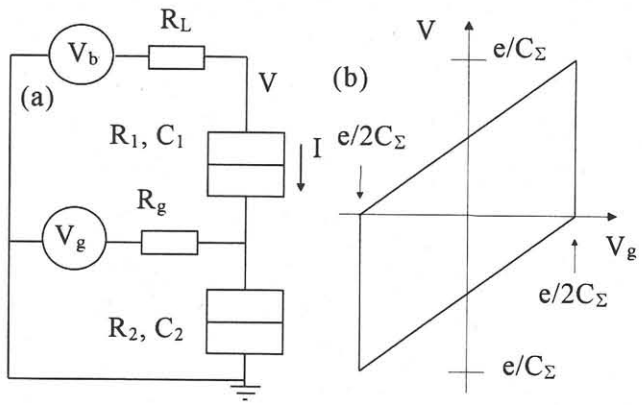

Fig.1. (a) Schematic layout of the R-SET and the measurement set-up; (b) Coulomb blockade region of the R-SET at T=0. No current flows through the circuit inside the blockade region.

Simulations of R-SET based on the orthodox theory were also carried out [6].

3. Results and discussion

Tunnel resistance of each junction can be extracted independently from the linear fit to their I-V curves in the voltage range 5 ~ 10 mV. This gives $R_1 = 76$ kΩ and $R_2 = 62$ kΩ. Gate resistor I-V curve was also fitted and gave $R_g = 1.71$ MΩ. Transistor capacitance can not be measured accurately in R-SET but a rough estimation can be obtained from the offset of high bias (up to about 20...30 mV) asymptotes of the I-V curve. Thus, $C_\Sigma \sim 300$ aF was deduced. As follows from the theory and confirmed by our simulations, it is only C_Σ which determines the shape of Coulomb blockade (see Fig.1b) and neither I-V nor V-V_g curves depend on the ratio C_2/C_1.

Sweeping V_b, we measured I-V curves at different gate voltages (the data is not presented here because of lack of space). When V_g is zero, the current is strongly suppressed at low bias. This fact indicates that despite a direct connection of a long metallic gate to the island, the stray capacitance of the gate does not contribute significantly to the total capacitance C_Σ. The current remains suppressed in the range $-0.2\ \text{mV} \leq V_g \leq 0.2\ \text{mV}$. Outside this range, the I-V curve becomes linear at zero bias. The dependence on the gate

voltage is non-periodic, once the blockade is lifted, it is never restored again in contrast to the C-SET where it is strictly periodic in gate charge.

The operation of the R-SET is clearly shown in Fig.2a where transfer curves (V-V_g) are presented for different bias voltages. The load resistor $R_L = 10$ MΩ was used. The step in bias voltage is 90 μV. At low V_b (two curves in the middle), there is a blockade-like feature in V-V_g dependence. Because of the offset in the measurement set-up, the curve does not go through the origin of the plot. Above certain bias voltage, $|V_b| \geq 200$ μV, the dependence becomes non-monotonic with a clear negative slope observable up to $|V_b| \approx 1.2$ mV. The negative slope is the most pronounced at a bias voltage $|V_b| \sim 350$ μV which should correspond to e/C_Σ of the transistor and where the highest K_v might be obtained. In our case $|K_v| \approx 0.2$ is measured, a factor of 30 smaller than what we expected to have with the above parameters [3]. One of the possible reasons for this is mentioned below.

Both measured I-V vs. V_g and V-V_g vs. V_b dependences seem to be in agreement with the predictions of the orthodox theory of single electron tunneling. In both of them, Coulomb blockade region was observed resembling the one in Fig.1b. To make a quantitative comparison, we simulated of V-V_g vs. V_b curves using e/C_Σ and $k_BT/(e^2/C_\Sigma)$ as fitting parameters (Fig.2b). While the first one was fixed for all the curves, we had to increase the second parameter from 0.02 at $V_b/(e/C_\Sigma) = 0$ up to 0.065 at $V_b/(e/C_\Sigma) = 4$. This corresponds to the bias dependent effective temperature of the R-SET 120 ~ 380 mK. Such a high effective temperature was apparently the main reason for the poor voltage gain realized. The analysis of overheating in the R-SET is beyond the scope of this work. We just refer to paper [7] where the overheating in a small metal island of C-SET is reported. We believe similar effect may occur in the R-SET.

The simulated curves reproduce fairly well the general shape of the Coulomb blockade, however, there are some deviations from the experiment. In the simulated curves, the peak is wider and the slope outside the Coulomb blockade

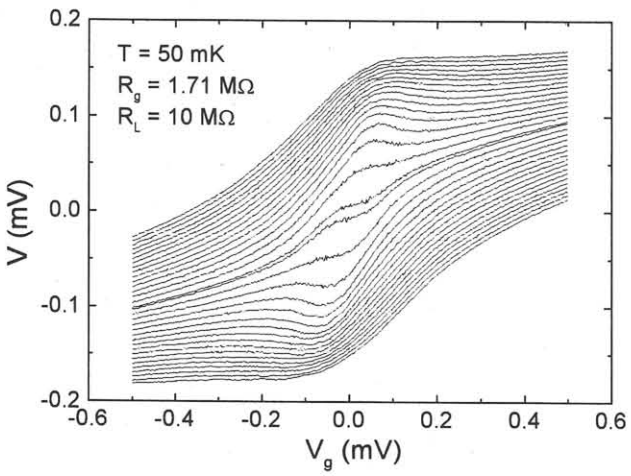

Fig.2a. Transfer curves of the R-SET taken at $V_b = 0, \pm 90$ μV, ± 180 μV, ...± 1440 μ.V

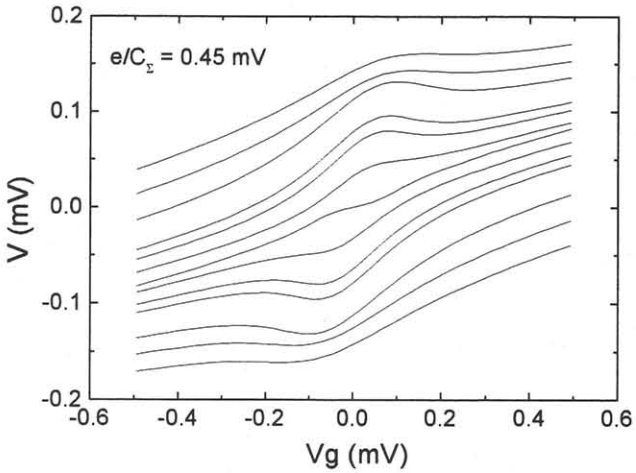

Fig.2b. Simulated V-Vg curves at $V_b/(e/C_\Sigma) = 0, \pm 0.3, \pm 0.7, \pm 1, \pm 2, \pm 3, \pm 4$. For these curves, we used $k_BT/(e^2/C_\Sigma) = 0.02$, 0.042, 0.043, 0.045, 0.05, 0.06, 0.065.

is somewhat smaller. We attribute this disagreement to the fact that the model we used is rather simple. In our model, the bias dependent contribution from the distributed stray capacitance of the gate to the C_Σ is not taken into account. Also, higher order tunneling processes (cotunneling) may be involved.

4. Conclusions

We fabricated and measured resistively coupled single electron transistor comprising two $Al/AlO_x/Al$ tunnel junctions and thin film Cr gate. Non-periodic Coulomb blockade pattern was observed in I-V and V-V_g curves. The operation of the R-SET is in good qualitative agreement with the orthodox theory of single electron tunneling. To obtain a high voltage gain, the parameter $k_BT/(e^2/C_\Sigma)$ must be decreased.

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* On leave from P. N. Lebedev Physics Institute, Moscow 117924, Russia

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