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Polycrystalline Silicon Single-Electron Transistor with Gate-Dependent Two-Period Current Oscillations

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1. Introduction

In recent years, the single-electron transistor (SET) has been extensively studied for future LSI device applications. In order to retain compatibility with CMOS process lines, SETs have been demonstrated in crystalline silicon-on-insulator (SOI) material [1]. Single-electron effects have also been observed at room temperature in an ultra-thin layer of re-crystallised amorphous silicon [2]. A polycrystalline silicon (poly-Si) SET has been demonstrated, with thermally grown oxide tunnel barriers sandwiched between poly-Si layers [3]. The use of poly-Si allows for greater process flexibility compared to crystalline silicon. In this work, we demonstrate single-electron tunnelling effects in heavily-doped poly-Si nanowire SETs, where the characteristics are dependent on the intrinsic granular nature [4] of the material. Since standard CMOS materials are used throughout the process, a simple SET/CMOS integration scheme is practicable.

2. Device Structure

The poly-Si material was prepared as follows. 50 nm-thick amorphous Si was deposited at 550 °C on 10 nm-thick gate quality oxide, thermally grown on a lightly-doped Si substrate. The amorphous Si was heavily-doped n-type (phosphorous, $3\text{-}4\times10^{19}/cm^3$) and annealed at 850 °C for 30 minutes to produce poly-Si with ~20 nm grains. The SETs consisted of poly-Si nanowires with two symmetrical side gates, defined using electron beam lithography and reactive ion etching. Thermal oxidation was used to thin and passivate the wires. Fig. 1 shows a scanning electron micrograph of a poly-Si SET wire of 20 nm × 30 nm active cross-section and 1 μm length. Such a nanowire is likely to be made up of a near 1-D chain of poly-Si grains. We have fabricated SETs with wire length from 200 nm to 1 μm for our experiments.

3. Results and Discussion

Fig. 2 shows single-electron tunnelling oscillations of the drain-source current with side gate bias in a poly-Si SET at 4.2 K. The oscillation period is ~90 mV for side gate bias from -0.5 V to 0.7 V. The period reduces sharply by a factor of 4.5 to ~20 mV for bias voltage greater than 0.7 V. We observed a similar transition in the oscillation period for positive bias close to 0 V in all devices which showed clear single-electron charging. In Fig. 3, the effect of single and double side gate biasing is shown on the oscillations in a second device. With a single side gate, the period reduces by a factor of 4.2 at ~0.6 V bias. With both side gates used together, the period reduces by a factor of 4 at ~0 V bias. Fig. 4 shows the temperature dependence of the oscillations in a third device. It is seen that the oscillations are smeared out by 15 K. Two-period oscillations are not observed in nanowire SETs fabricated in crystalline SOI material, where doping fluctuations create multiple tunnel junctions [1]. We propose that in poly-Si nanowires at low temperature, the grains and grain boundaries form islands and tunnel barriers which give rise to Coulomb blockade in electronic transport through the wire and oscillations in the current as a function of gate bias. The effect of the gate on a dominant charging island is influenced by electrostatic screening at the grain boundary states and changes in the occupancy of these states will modulate the effect of the gate bias on the island. An abrupt change in the current oscillation period is observed if a step exists in the energy distribution of the grain boundary states.

Although these devices only operate up to 15 K, it may be possible to raise this temperature to 77 K using poly-Si material with smaller grains and a different doping concentration. At this temperature, it is possible to integrate the SET with CMOS circuitry in memory arrays and logic circuits.

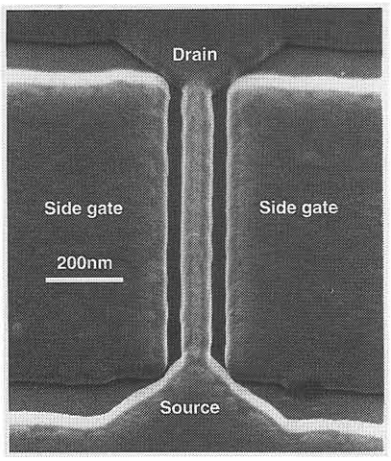

Fig. 1. SEM micrograph at 45° tilt of a nanowire SET fabricated in 50 nm thick poly-Si. The wire has been thermally oxidised, leaving an active wire width of 20 nm.

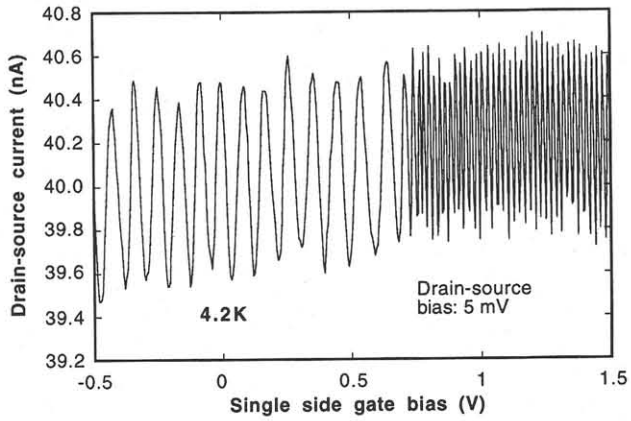

Fig. 2. Two-period oscillations of the drain-source current with side gate bias in a poly-Si SET at 4.2 K. The oscillation period changes sharply by a factor of 4.5 at 0.7 V gate bias.

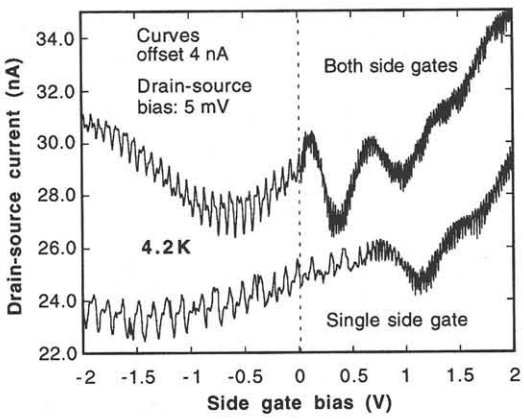

Fig. 3. Drain-source current oscillations at 4.2 K in a poly-Si SET using only a single side gate and using both side gates together. The oscillation period changes sharply for positive bias close to 0 V in either case.

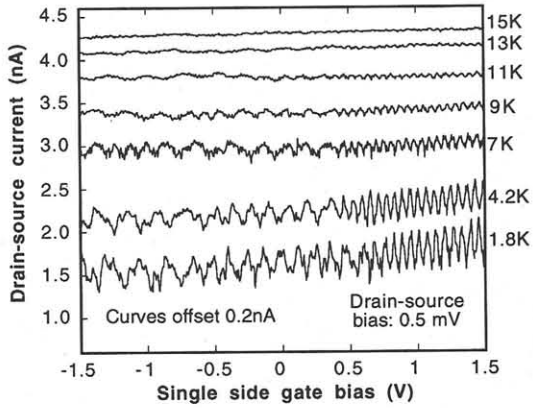

Fig. 4. Drain-source current oscillations with side gate bias in a poly-Si SET as a function of temperature. The oscillations smear-out by 15 K.

References

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