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**Invited**

# Strain Engineering of Silicon-Based Heterostructures: Materials and Devices

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## 1. Introduction to Strain Engineering

The introduction of biaxial tensile strain by epitaxial growth of thin Si layers on relaxed $Si_{1-x}Ge_x$ has a number of beneficial effects on bandstructure and transport in Si, including a conduction band offset and increased mobilities for electrons and holes. $Si_{1-y}C_y$ grown on Si also experiences tensile strain. In this work, we compare measurements of the MOS electron mobility and band offsets for the strained Si/relaxed $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$/Si materials systems.

Fig. 1(a) illustrates the *equilibrium* lattice constants $a_o$ for random $Si_{1-y}C_y$ alloys, Si, and $Si_{1-x}Ge_x$. The lattice mismatch to Si, $m = 100 \cdot (a_o(alloy) - a_o(Si))/a_o(Si)$, is – 20 % for $Si_{0.5}C_{0.5}$ and + 2 % for $Si_{0.5}Ge_{0.5}$. During growth, if the overlayer is sufficiently thin, the in-plane lattice parameter of the epitaxial layer is either contracted or stretched to match that of the substrate (Fig. 1(b)). If $a_o(overlayer) < a_o(substrate)$, the overlayer experiences biaxial tensile strain. This distortion produces an energy splitting, $\Delta E_s$, of the six-fold degenerate Si conduction band ($\Delta_6$) into two-fold degenerate ($\Delta_2$) and four-fold degenerate ($\Delta_4$) states (Fig 1(c)). $\Delta E_s$ is directly proportional to the lattice distortion and is given by $\Delta E_s \sim 165$ meV/(% mismatch). For strained Si on relaxed $Si_{1-x}Ge_x$, $\Delta E_s \sim 660 \cdot x$ (meV), where $x$ is the Ge fraction in the substrate, and for $Si_{1-y}C_y$ on cubic Si, $\Delta E_s \sim 66 \cdot y$ (meV). For tensile strain, the $\Delta_2$ band is lower in energy than $\Delta_4$, and hence is preferentially occupied by electrons. Intervalley scattering is thus reduced, which results in a mobility enhancement. In addition, the energy of $\Delta_2$ is lowered by $(2/3)\Delta E_s$ with respect to $\Delta_6$ (Fig. 1(d)), which can contribute significantly to the conduction band offset.

## 2. Mobility Enhancements in Strained Si MOSFETs

Calculations predict that even in the deep submicron regime, enhancing channel mobility improves MOSFET transconductance [1], in contrast to the conventional notion of strict electron velocity saturation. Mobility enhancements in surface-channel strained Si *n*-MOSFETs have previously been reported for low substrate doping, i.e. low vertical effective fields, $E_{eff}$ (Fig. 2, open symbols) [2]. Strained Si epitaxial layers were grown on graded, relaxed $Si_{1-x}Ge_x$ buffer layers ("substrates") by chemical vapor deposition. Varying the substrate Ge content produced devices with different amounts of strain in the Si channel. As the tensile strain in the Si is increased, the electron mobility, $\mu_{eff}$ is enhanced by up to 80% compared to that in CZ Si control devices. The strain dependence of the measured mobility enhancement is in good agreement with theoretical predictions for strained Si MOS inversion layers [3]. Our recent results (Fig. 2, closed symbols) indicate that this mobility improvement persists for high $E_{eff}$ (~1 MV/cm) in highly-doped structures suitable for operation at channel lengths of 0.1 μm [4]. As conventional Si MOSFETs are scaled, the vertical effective field increases and the mobility decreases according to the universal relationship, $\mu_{eff}(E_{eff})$ (Fig. 2, dashed line [5]). Strain provides a means of moving off of this curve, and thus overcoming limitations imposed by the fundamental trade-off between device speed and short-channel effects. In addition to the improvements in electron transport, hole mobility enhancements have been demonstrated in strained Si *p*-MOSFETs [6,7], as the tensile strain also splits the valence band degeneracy.

## 3. New Materials: Strained $Si_{1-y}C_y$ on Si

Tensile strain can be introduced without a relaxed buffer layer by the addition of a few percent C to Si. High-resolution x-ray diffraction (XRD) data (Fig. 3) demonstrates the variation from compressive ($Si_{1-x}Ge_x$) to tensile ($Si_{1-y}C_y$) strain for layers grown by chemical vapor deposition (CVD). Good agreement between the simulated and measured XRD indicates high structural quality. A key issue for synthesis of $Si_{1-y}C_y$ alloys is the low equilibrium solubility of C in Si. Fig. 4 compares substitutional to total C concentrations for both $Si_{1-y}C_y$ and $Si_{1-y}Ge_xC_y$ [8,9]. For low growth temperatures (550°C), the C is fully substitutional, to within experimental error, for C concentrations up to ~ 1.8 at. %.

*n*-MOSFETs employing strained $Si_{1-y}C_y$ channels have been fabricated [10]. Low-temperature plasma-enhanced CVD gate oxides were used to reduce thermal exposure of the strained $Si_{1-y}C_y$. Fig. 5 summarizes measured effective electron mobility for C contents up to 0.8 at. %. In contrast to tensile-strained Si, no electron mobility enhancement is observed for $Si_{1-y}C_y$ *n*-MOSFETs. These preliminary results indicate that alloy or other scattering mechanisms may be compensating the potential beneficial impact of strain on electron mobility in $Si_{1-y}C_y$. However, an exciting prospect for these materials is the presence of a conduction band offset, which is lacking for compressively strained $Si_{1-x}Ge_x$/Si. Fig. 6 summarizes the $Si_{1-y}C_y$/Si conduction band offsets extracted from MOS *C-V* analysis [11]. An energy offset of 100 meV is measured for 1.6 atomic % C.

## 4. Conclusions

Strained Si/relaxed $Si_{1-x}Ge_x$ can be used to improve mobility at a given $E_{eff}$, and to enhance transconductance in surface-channel MOSFETs. Although the expected strain-induced mobility enhancement was not observed in $Si_{1-y}C_y$ channel *n*-MOSFETs, the $Si_{1-y}C_y$/Si conduction band offset is promising for a number of applications, including quantum-effect devices and heterojunction bipolar transistors.

Acknowledgments

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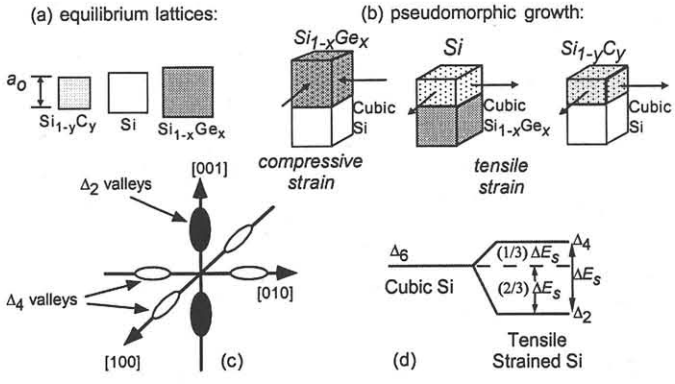


**Fig. 1.** Schematic (a) equilibrium lattices and (b) pseudomorphic growth. The (c) constant energy diagram and (d) conduction band energy splitting is shown for tensile strained Si.

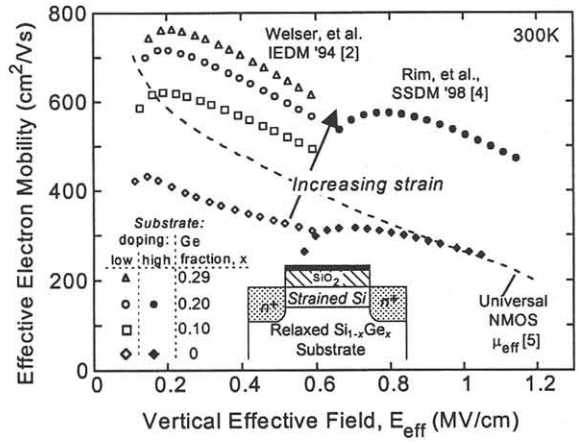


**Fig. 2.** Measured electron mobilities versus effective field, $E_{eff} = (Q_{dpl} + (1/2)\cdot Q_{inv})/\varepsilon$. Inset shows the strained Si MOSFET structure. The strained Si layer is ~ 10 nm thick.

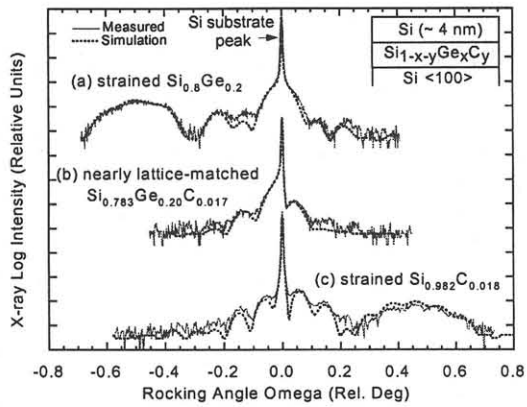


**Fig. 3.** High resolution XRD (004) rocking curves for (a) 27 nm-thick $Si_{1-x}Ge_x$, (b) 24 nm-thick SiGeC, and (c) 22 nm-thick $Si_{1-y}C_y$ epitaxial layers grown at 550°C by CVD.

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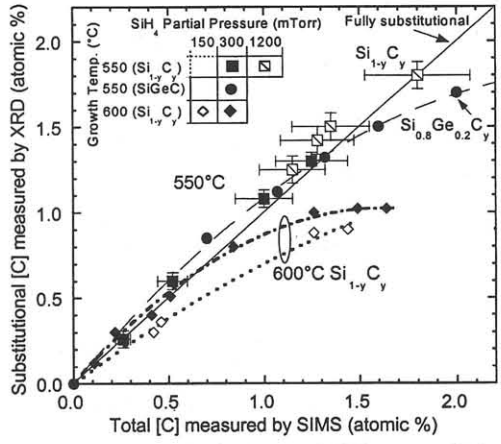


**Fig. 4.** Comparison of substitutional [C] extracted from XRD to total [C] measured by secondary ion mass spectrometry (SIMS) for $Si_{1-y}C_y$ and SiGeC epitaxial layers grown by CVD.

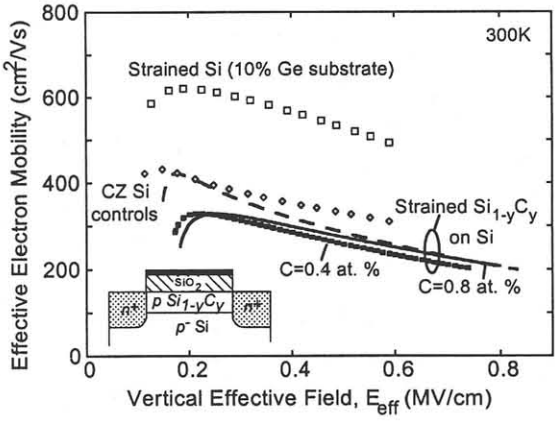


**Fig. 5.** Measured electron mobilities for strained Si/relaxed $Si_{1-x}Ge_x$ (□) and $Si_{1-y}C_y$/Si (lines) *n*-MOSFETs.

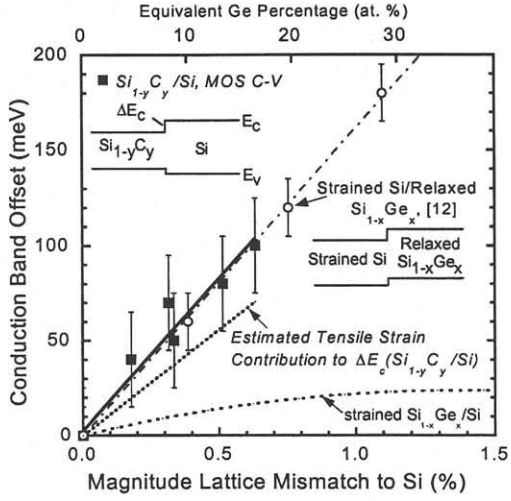


**Fig. 6.** Conduction band offsets for strained Si/relaxed $Si_{1-x}Ge_x$ (○) and $Si_{1-y}C_y$/Si (■), where *[C] (at. %) = mismatch(%)/0.395.*