RF Noise Study of Small Gate Width Si-MOSFETs up to 8GHz Application for Low Power Consumption

E. Morifuji, C. E. Biber*, W. Bachtold*, T. Ohguro, T. Yoshitomi, H. Kimijima, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai
Toshiba Corporation, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210-8582 Japan,
TEL:+81-44-549-2335, Fax:+81-44-549-2213, E-mail:morifuji@sdl.rdc.toshiba.co.jp
* Swiss Federal Institute of Technology (ETH) Zurich

Introduction

Recently, high performance RF analog CMOS devices for 2GHz telecommunication equipment has shown remarkable progress and reported by several groups[1]-[8] as shown in Table I. Already fT values of more than 150 GHz have been reported for sub 0.1 μm gate length n-MOSFETs [1][2]. In the 0.1 - 0.3 μm gate length range, 35 GHz - 120 GHz for fT, 28 GHz - 46 GHz for fmax, and 0.4 dB - 0.8 dB for NFmin were demonstrated. However, in general, gm of MOSFETs is smaller than that of GaAs and bipolar transistors. Thus, large gate width such as 200 - 1,000 μm has been used for obtaining the high gain comparable to those of bipolar. By downsizing the gate length, high gm will be achieved and thus the gate width could be decreased. This is good in terms of power consumption of the circuit.

The purpose of this paper is to study the gate width dependence of noise figure of 0.25 - 0.13 μm gate length RF CMOS transistors, and to show sufficiently high performance of smaller gate width devices not only for 2 GHz operation but also for 5-8 GHz operation with low power consumption.

Sample fabrication

Figure 1 shows the cross section of the RF CMOS used in the experiments. In-situ phosphorous doped poly Si was used for the gate electrode of both n- and p-MOSFETs. Co SALICIDE was adopted to MOSFETs in order to reduce the gate/source/drain resistance. The gate electrode is divided 5 μm length pieces by adopting multi-finger layout.

AC measurement Results and Discussions

Figures 2 and 3 show the measurement results of the gate width dependence of fT and fmax. The gate length is 0.18μm. With decrease in gate width, fT and fmax curves shift to the lower current direction without degradation in fT and fmax values. This means that we can downsize the gate width to achieve low power operation without the sacrifice of fT and fmax values.

The measurement results of the gate width dependence of NFmin at 5GHz operation is shown with open symbols in Figure 4 . It should be noted that NFmin value shows the significant degradation, when the gate width is downsized. As shown in Figure 5, the AC current path from the bonding pad via the substrate to the ground exists. Thus, an additional thermal noise source composed of substrate resistance is connected at the input stage of MOSFETs and is expected to have a significant influence on the NFmin characteristics. In real circuit, the current path via the bonding pad can be suppressed by several techniques. The additional component can be de-embedded by removing the parasitic components of the noise correlation admittance matrix [Cy]open from that of the total matrix [Cy]total as shown in Fig. 5[10]. The de-embedded results are shown with filled symbols in Fig. 4. Very small NF values comparable to that of GaAs device(Table I) have been obtained for the intrinsic portion of Si-MOSFETs for the first time. It was confirmed that we can reduce the drain current and power consumption by reducing the gate width without degrading the NFmin characteristics in the de-embedded case.

In the case of NFmin, matching between the input and MOSFET has to be taken perfectly by inserting the matching circuit. On the other hand, NF50 value (noise figure value in the case input stage is connected to 50Ω) is another figure to predict the worst case without the matching circuit, and it is also important to know the behavior of NF50.

Figure 6 shows the dependence of NF50 on the gate width of n-MOSFETs for 5GHz. The drastic degradation of NF50 caused by the downsizing of gate width is observed in non-de-embedded case shown with open symbols. Although the degradation is considerably suppressed by de-embedding as shown by filled symbols, the NF50 values increase with gate width decrease.

Figure 7 shows the equivalent circuit for MOSFETs. NFmin can be expressed as Eq(1) as shown in figure 7, which suggests NFmin has no dependence on gate width. This agrees with the measurement results in Figure 4. In general, the NF value is expressed as Eq(2) as shown in Figure 8. From this, NF50 is expressed as Eq(3). In Table II, each term in Eq(3) on various gate widths is shown. The narrower gate width MOSFET has larger Rn value in inverse proportion to gate width Wg as shown by Eq(4) in Figure 8(Other terms except Rn do not change significantly.). This causes the degradation of NF50. The situation can be understood by the noise circles plotted in Figure 8. Thus, it will be a key to provide a good noise matching in the small gate width MOSFETs used for the purpose of the low power consumption.

Figure 9 shows the dependence of fT, fmax, and NFmin on the gate length of n-MOSFETs with tox = 4.5 nm. These AC characteristics improve by reducing the gate length thanks to the increase in gm. Non-de-embedded data are also plotted for NFmin case.

AC characteristics of the n-MOSFETs for various generation are measured by using the de-embedded technique(as shown in Table III). The advanced generation device has high gm value because of short gate length and thin gate oxide. This benefits fT, fmax, and NFmin values. Very low NFmin value comparable to that of GaAs device has been obtained at higher frequency of 5 and 8 GHz in the intrinsic part of MOSFETs. Improvement of the fmax value is slightly smaller than that of fT. Some kind of process optimization such as raised source, gate, and drain structure[11] would be desirable to further improve this.

Conclusion

We have shown for the first time by using the de-embedded technique that the intrinsic Si-MOSFET NFmin is as good as a few 0.1dB even at high frequency 5-8GHz. This low NFmin value can be kept with decrease in gate width for the purpose of low power consumption. On the other hand, NF50 increases with decrease in the gate width. Thus, development of the on-chip matching technique will become critically important for low power RF CMOS with small gate width. It can be expected that high performance RF circuit with low noise and low power would be realized by making use of the excellent intrinsic noise performance of Si MOSFETs here.

References

[1]C.Wann, et al., IEEE EDL, NO.12, 1997, p.625
[2]H.S.Momose, et al., IEEE IEDM Tech. Dig., 1996, p.105
[3]A.Chatterjee, et al., IEDM Tech. Dig.,1997, p.821
[4]D.Hisamoto, et al., 1996 Symp. on VLSI Tech., p.104
[5]T.C.Holloway, et al., 1997 Symp. on VLSI Tech., p.13
[6]D.Eggert, et al., IEEE Trans. on ED, NO.11,1997, p.1981
[7]T.Ohguro, et al., 1996 Symp. on VLSI Tech., p.132
[8]H.Shimomura, et al., 1997 Symp. on VLSI Tech., p.73
[9]K.Onda, et al., 1993 Proceedings of Int. Symp. GaAs and Related Compounds, p.15
[10]H.Hillbrand, et al.,IEEE Trans. on CAS,NO.4, 1976, p.235
[11] T.Ohguro, et al., 1998 Symp. on VLSI Tech., to be presented

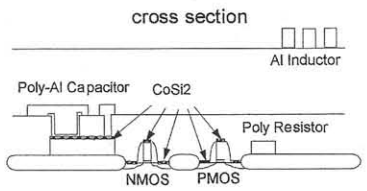


Fig.1 Co-salicided analog CMOS structure

	Device	Lg [μm]	Wg [μm]	Tox [nm]	fT [GHz]	fmax [GHz]	NFmin. @2GHz	ref.
Si	NMOSFETs	0.07	—	2.7	150	—	—	[1]
	NMOSFETs	0.09 0.12	200 1000	1.5	150	— —	— 0.5dB	[2]
	NMOSFETs	0.10	256	2.0	120	28	0.5dB	[3]
	NMOS(SOI)	0.14	200	—	40	—	0.8dB	[4]
	NMOSFETs	0.18	—	4.0	72	28	0.55dB	[5]
	NMOS(SOI)	0.20	400	10.0	23	46	0.7dB	[6]
	NMOSFETs	0.20	200 1000	4.0	42 —	— —	0.6dB 0.4dB	[7]
	NMOSFETs	0.30	200	—	35	37	0.6dB	[8]
GaAs	InAlAs/InGaAs FET	0.15	100	—	185	—	0.2dB	[9]

Table I Priviously reported AC characteristics of MOSFETs

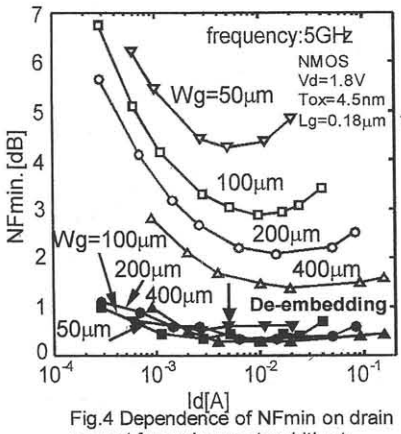


Fig.4 Dependence of NFmin on drain current for various gate width at 5GHz operation.

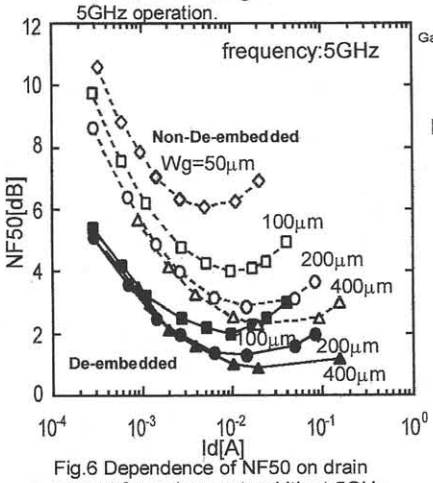
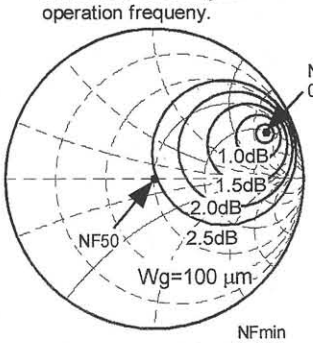
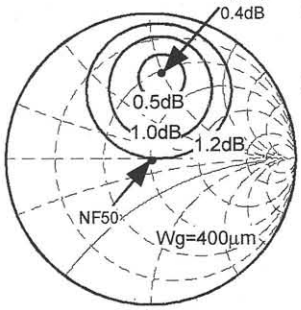
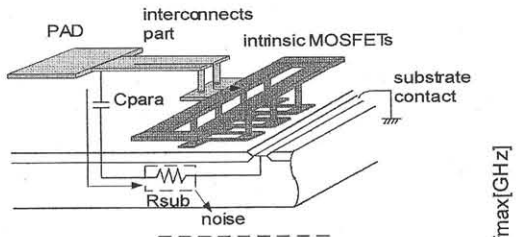
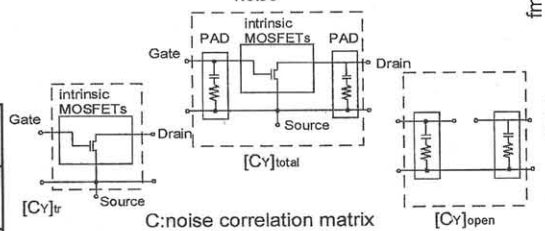


Fig.6 Dependence of NF50 on drain current for various gate width at 5GHz operation frequeny.









C:noise correlation matrix

[CY]total :obtained by transformation from [CA]total

[CA]total :determined by noise measurement

$$[CA]_{total} = 2kT \begin{bmatrix} Rn & \frac{NFmin-1}{2} - Rn\overline{Yopt} \\ \frac{NFmin-1}{2} - RnYopt & Rn|Yopt|^2 \end{bmatrix}$$

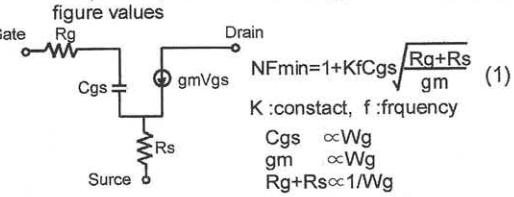
Rn:equivalent noise resistance, Yopt:optimal input admitance

[CY]open: determined by s-parameters on open pattern

$[CY]_{open} = 2kT\,Re[Y]$

$[CY]_{tr} = [CY]_{total} - [CY]_{open}$

Fig.5 Mechanism of NF degradation caused by parastic components, and de-embedding procedure on noise figure values



$$NFmin = 1 + KfCgs\sqrt{\frac{Rg+Rs}{gm}} \quad (1)$$

K :constact, f :frquency

Cgs ∝Wg

gm ∝Wg

Rg+Rs∝1/Wg

Thus NFmin = 1+K1f

(independent of gate width(Wg))

Fig.7 Equivalent circuit and NFmin expression for MOSFETs

Noise Circle

$$NF = NFmin + \frac{4Rn|\Gamma s - \Gamma opt|^2}{(1-|\Gamma s|^2)|1+\Gamma opt|^2} \quad (2)$$

$$NF50 = NFmin + \frac{4Rn|\Gamma opt|^2}{|1+\Gamma opt|^2} \quad (3) \quad (\Gamma s=0)$$

Rn :equivalent imput noise resistance

Γopt :reflection coeficient at NF=NFmin

Rn=Q/gm∝1/Wg (4)

Q:constant

(dependent on gate width(Wg))

Fig.8 Noise circle for various gate width (Frequency:5GHz, Lg=0.25μm nMOSFETs Vg=V@gmmax)

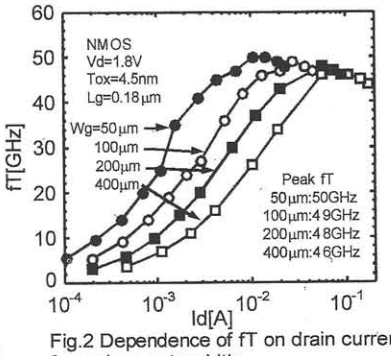


Fig.2 Dependence of fT on drain current for various gate width

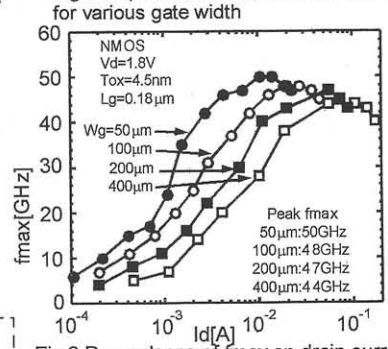


Fig.3 Dependence of fmax on drain current for various gate width

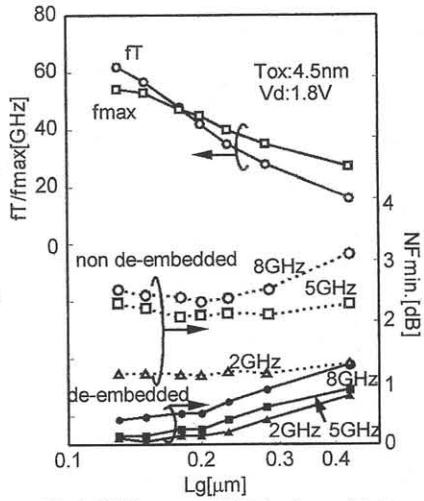


Fig.9 fT, fmax, and NFmin dependence on gate-length(Lg)

Wg[μm]	Rn[Ω]	$\|\Gamma opt\|^2/\|1+\Gamma opt\|^2$	$\|\Gamma opt\|$	$\angle\Gamma opt$(rad)
100	48	0.21	0.82	0.43
200	25	0.21	0.76	0.77
400	12	0.29	0.66	1.53

Table II Noise parameters defined in equation(3)

Lg [μm]	Tox [nm]	VDD	fT [GHz]	fmax [GHz]	NFmin[dB] @5GHz	NFmin[dB] @8GHz
0.13	3.0	1.2	76	55	0.1	0.3
0.15	4.0	1.5	55	53	0.2	0.3
0.18	4.5	1.8	49	48	0.3	0.4
0.20	5.0	2.0	45	44	0.3	0.5
0.25	6.0	2.5	43	42	0.4	0.7

Table III AC characteristics for various generation NMOSFETs(Wg=200μm)