Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 84-85

Invited

Modeling and Characterization for Ultra Deep Submission CMOS Devices

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I. Introduction

As we move into 21st century, ultra-deep submicron (UDSM) CMOS technology with feature size of 0.1μm or less will become in common use. Although at these dimensions, the path delay due to interconnections takes over the device gate delay, accurate modeling of the active devices is still very important. This is particularly so in mixed digital/analog designs and/or applications involving low power supply voltage.

Basically there are three approaches of modeling CMOS transistors that are commonly used in SPICE like circuit simulator [1]. These are (1) regional approach wherein different equations for different regions of device operation are pieced together by smoothing functions to avoid discontinuities [2]-[5], (2) surface potential (ϕ_s) based approach which is inherently continuous but require iterations to solve for ϕ_s at each bias point [6]-[7]. A third approach that is based on *a priori* generating current and charges as a function of operating voltages for different W/L (width/length) is often used at full chip level simulation to achieve fast execution time.

In this paper we will discuss advantages/disadvantages of different modeling approaches and suggest a new modeling approach that is more appropriate for UDSM MOSFETs.

II. Hybrid Approach

The most commonly used regional based MOSFET models have the following deficiencies; (1) Large number of adjustable parameters, some of which may be correlated, thus complicating the parameter extraction process. (2) Error in the moderate inversion region, an important device operation region for analog design, is often very large. (3) Discontinuities in the derivatives of current and charges at the boundary between forward and reverse mode of operation. (4) Scalability over full range of available geometries (W/L) normally not possible without restoring to parameter "binning". However, the advantage is that device physical effects can easily be incorporated through empirical relations.

The above short comings of regional based models are removed using surface potential based approach that describes the full operating range from weak to moderate to strong inversion in a physical and continuous way without restoring to parameter "binning" and with fewer number of easily extractable parameters. However, the main drawback of this approach is compute time due to iterations required to calculate ϕ_s. Also short-channel effects are not easy to implement.

A better approach of MOSFET modeling applicable to UDSM technologies is the so called *hybrid approach*, which combines regional and surface potential approaches to take advantages of both approaches. In the hybrid approach surface potential at the source end is calculated in the usual way, while at the drain end one assumes $\phi_{sL} = \phi_{s0} + V_{dsx}$, where $V_{dsx} = f(V_{ds}, V_{dsat})$ is the the drain voltage V_{ds} that moves to V_{dsat} in a continuous way [1]-[3]. This approach results in the drain current

$$I_{ds} = \frac{\mu_s W C_{ox} \left(V_1 + \alpha V_t - 0.5\alpha V_{dsx}\right) V_{dsx}}{L - l_d + \delta_0 \mu_s V_{dsx}/\nu_{sat}} \qquad (1)$$

where $V_t = kT/q$ is thermal voltage, α describes the bulk charge and $V_1 = Q_i/C_{ox}$ is a function of surface potential as

$$V_1 = \gamma u / \left[\sqrt{f\phi_s - V_t + u} + \sqrt{f\phi_s - V_t}\right] - \Delta V_1{}^{poly} \qquad (2)$$

where γ is a body factor, f is position independent lateral gradient factor [6]

$$f = 1 - \left(\epsilon_{si}/qN_{sub}\right)\partial^2\phi/\partial y^2 \qquad (3)$$

where N_{sub} is substrate doping concentration,

$$u = V_t \exp\left[\left(\phi_s - 2\phi_f - V_{sb}\right)/V_t\right]$$

Last term in (2) describes voltage drop in polysilicon depletion layer [3].

Equation (1) incorporates all the essential device physics of scaled devices such as short and narrow width effects, reverse short-channel effect (RSCE), bias dependent S/D series resistance (R_s), velocity saturation ν_{sat}, channel length modulation (CLM) etc. Note that eq. (1) is similar to regional based models but the concept of threshold voltage and charge sharing is not invoked. The effect of R_s is included through effective mobility term μ_s. The CLM effect is described through l_d, while drain induced barrier lowering (DIBL) and short channel effect are introduced through function f. The RSCE is described through flatband voltage [1].

It is found that (1) could be used to simulate I-V characteristics down to 0.1 μm fairly accurately, although at the expense of some non-physical parameters such as gate oxide thickness t_{ox}. Figure 1 shows measured (symbols) and simulated (lines) I-V characteristics of 0.1 μm device

fabricated using X-ray lithography [8]. The average error between measured and simulation is less than 4%. To fit this data t_{ox}=53Å is used, while physical t_{ox} is 45Å as measured using procedure discussed in [9]. One set of parameters (total of 27) fits all device sizes from 0.1μm to 1 μm for which data was available.

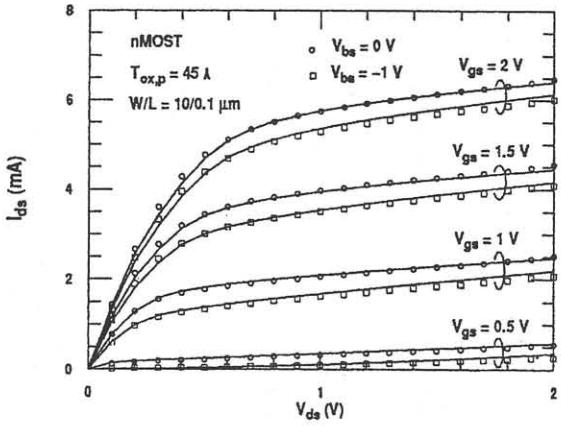

Fig. 1: Fit to drawn characteristics of an nMOST with L=0.1 μm. Full lines Eq. (1), symbols, measured data.

III. Quantization Effect

As devices are being scaled towards 0.1μm dimensions, gate oxide thickness is decreasing (20-30 Å) while channel doping is increasing (6-8x10^{17} cm^{-3}) to achieve the desired device turn-off and drive current. This leads to quantization of the accumulation/inversion layer resulting in the charge centroid of the layer to move away from the Si-SiO_2 interface by 20-30 Å [9]-[10]. Thus finite thickness of the inversion/accumulation layers can no longer be neglected, and must be taken into account while calculating C_{ox} required in (1). This explains why one need to use t_{ox}=53 Å, rather than 45 Å in fitting data of Figure 1. C_{ox} calculated which is order of the t_{ox}. This quantization effect could be included in (1) through change in ϕ_s, such that

$$\phi_s = \phi_s{}^0 + \Delta\phi_s{}^{qm} \qquad (4)$$

where $\Delta\phi_s{}^{qm}$ is the change in surface potential due to quantization effect and is proportional to increase in energy gap of silicon (δE_g) at Si-SiO_2 interface. Note that $\Delta\phi_s{}^{qm}$ in accumulation and inversion layers will be different and need to be pieced together unless some continuous function is developed. Using a simplified expression for δE_g [11], we find that one gets a fit similar to shown in Figure 1, but with t_{ox}=45Å.

Using this model capacitances become more accurate, although one needs to use bias dependent overlap capacitance [3] while fitting capacitance data with the models shown in Figure 2. In fact without (4) one can not achieve accurate moderate inversion fit. This figure also shows impact of polydepletion effect.

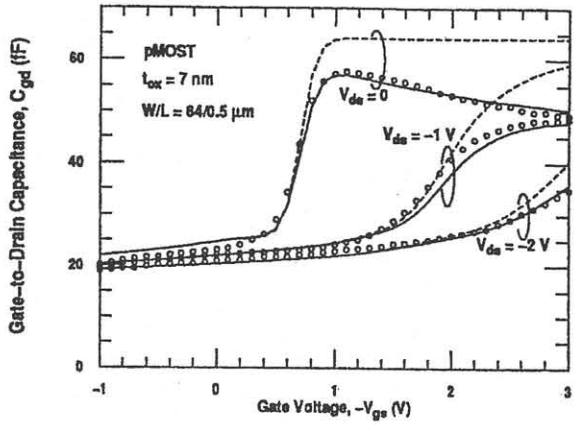

Fig. 2: Comparison of measured (circles) pMOST C_{gd} with (solid line) and without (dashed lines) polydepletion model ($\Delta V_1{}^{poly}$).

At 0.1μm dimensions effect of self heating and velocity overshoot might also be needed, but even without those two effects model discussed above work very well.

IV. Parameter Extraction

Parameter extraction is an important part of the model development [1]. The parameter extraction depends not only on the number of parameters but also on the model characteristics. Fewer the number of parameters easier it is to extract their values. It is advisable that parameters should be first extracted from regions of operation where they have more influence, while keeping physical meaning of the parameter, and then globally fitting the data to full curve.

V. Conclusions

Different MOS transistors modeling approaches are reviewed and a hybrid approach, that includes quantization of inversion layer, is proposed.

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