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Stress-Induced Device Degradation Due to Die-Attach Process after Area Bump Formation

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I.Introduction

Along with the increase in LSI speed and in the level of LSI circuit integration, there has been a rapid increase in the number of chip I/O connections and the size of packages. Area bump technology is solution because it allows wire-less and/or lead-less interconnection and full surface flip-chip interconnection. In the area bump process, a number of bumps are fabricated directly on the device region of an LSI chip. However, it has been reported that bond pads crack and that Si-nodules on oxide underneath the aluminum pads are generated by bonding stress during the wire bonding process[1]. We have investigated the influence of stud bumping above the device region on device reliability[2] and have found that gm degradation increases with increasing stud bump bonding force for N-channel MOSFETs and the degradation can be completely eliminated by terminating the dangling bonds with hydrogen atoms. After stud bump formation, the packaging process is performed in order to connect the LSI chip and die, and it seems that this process induces stress directly on the device region again.

In this paper, we discuss stress-induced device degradation due to the die-attach process after area bump formation. Next, the effect of post-baking after attaching the die on the degradation is investigated. Finally, ways to suppress device degradation due to the packaging process are suggested.

II. Sample Preparation and Experimental Procedures

The processes for fabricating the area bump and forming the package are shown in Fig. 1. The devices were N-channel (N-ch) MOSFETs with an LDD structure. The poly-Si gate was 0.5-μm long and 20-μm wide and the thickness of the gate oxide was 11 nm. After device fabrication, a stud bump, a gold ball about 90 μm in diameter, was formed above the MOSFET region as shown in Fig. 1(a). Then hydrogen annealing at 400 °C for 30 min was performed to eliminate the device degradation due to the stud bump[2]. Next, a die was aligned face-to-face with the gold bumps and attached by applying pressure as shown in Fig. 1(b). In the die-attach process, the pressure was 1 - 5 Kg. Then, after pre-heating at 180 °C for 30 min, the potting process was performed as shown in Fig. 1(c). Conventional potting material was used in this study. The final step was post-baking at 180 °C for a few hours. Stress due to the die-attach process was calculated from pressure and the total area covered by the balls. Device degradation was evaluated by measuring V_{th} and the maximum value of gm at V_D = 0.1 V. Using the charge pumping method, we also estimated the interface trap generation.

III. Results and Discussion

A. Device degradation due to stress

Figure 2 shows the maximum gm degradation rate ($\Delta gm/gm0$) as a function of the stress. The gm0 is the value before packaging process. The gm degradation linearly increased with increasing stress. A 20-percent order of gm degradation rate was observed after stress at 150 MPa. The relationship between the V_{th} shift and stress is shown in Fig. 3. The amount of V_{th} shift also increased with increasing stress and a 100-mV order of V_{th} shift was observed after stress at 100 MPa. Figure 4 shows the change in the maximum charge pumping current, ΔI_{cp}, as a function of stress. Although ΔI_{cp} increased with increasing stress, it saturated at 150 MPa. In order to investigate the relationship between the stress and device degradation in detail, we examined the subthreshold characteristics before and after packaging. Figure 5 shows that the subthreshold slope changed between at 100 MPa, indicating that interface traps were generated at the Si-SiO_2 interface in the MOSFETs. Moreover, as shown in Fig. 5(c), the change in the subthreshold characteristics at 175 MPa is mainly a parallel shift along the V_G axis. This means that electron-trap centers are generated in the gate oxide of the MOSFETs. These results suggest that the stress induced by the die-attach process,when low, mainly generates interface traps at the Si-SiO_2 interface in MOSFETs and, when high, causes the trap level lowering that is associated with mechanical stress[3] and observed as large ΔV_{th}.

B. Annealing effect

In spite of the post-bake at 180 °C for a few hours, device degradation due to the stress appeared. To investigate the relationship between baking temperature and device degradation, annealings were performed in air at T = 100 - 300 °C. Figure 6 shows the annealing effect on the stress dependence of the V_{th} recovery rate. The V_{th} recovery rate, Recov(V_{th}), is defined by

$$\mathrm{Recov}(V_{th}) = \frac{V_{th}(\mathrm{Pack}) - V_{th}(\mathrm{Anneal})}{V_{th}(\mathrm{Pack}) - V_{th}(\mathrm{ini})} \times 100(\%) \qquad (1)$$

where V_{th}(Pack), V_{th}(Anneal), and V_{th}(ini) are values of V_{th} after packaging, after annealing, and before packaging, respectively. The V_{th} shift due to the stress was not completely eliminated below 250 °C but was eliminated at 300 °C. This tendency is the same as the recovery of gm characteristics. It seems that the recovery of V_{th} is mainly a result of electron detrapping and that the recovery of gm is due to the restructuring of the weak Si-O bonds broken by stress.

Figure 7 shows the dependence of device degradation after annealing on time. Both gm degradation and V_{th} shift increased with the passage of time. This indicates that device degradation due to the potting material appears after the post-bake. Therefore, for suppression of device degradation due to the packaging process, we must consider both the post-bake condition and potting material .

IV. Summary

Device degradation increases with increasing stress induced by the die-attach process. It has been clarified that the device degradation due to this process results mainly from interface-trap generation as well as from enhanced electron trapping. This degradation is eliminated by post-baking at 300 °C. However, the degradation due to the potting material appears after the post-bake again. Therefore, we conclude that when packaging technology with area bump formations used, the post-bake condition and potting material are the most important factors affecting device reliability.

References

[1] T. B. Ching, et al., Proc. IRPS, p. 64, 1988.
[2] N. Shimoyama, et al., Proc. IRPS, p.118, 1997.
[3]A. Hamada, et al., Symposium on VLSI Tech., p. 98, 1992.

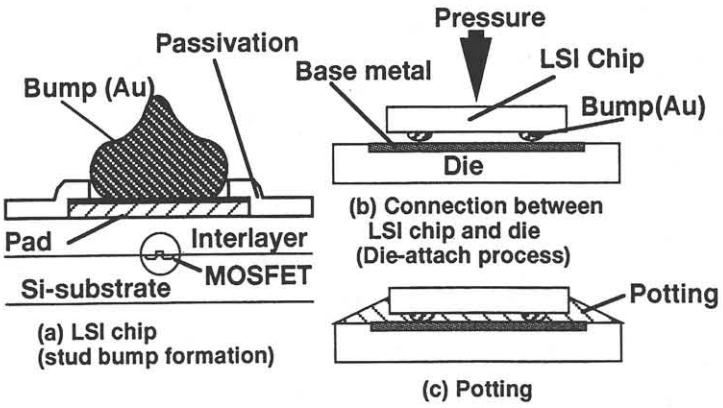

Fig. 1 LSI chip and packaging process

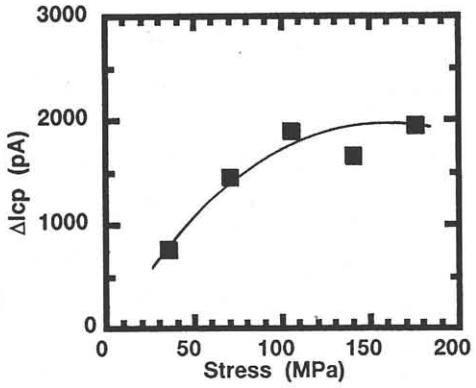

Fig. 4 Dependence of the change in the maximum I_{cp} on the stress induced by the die-attach process.

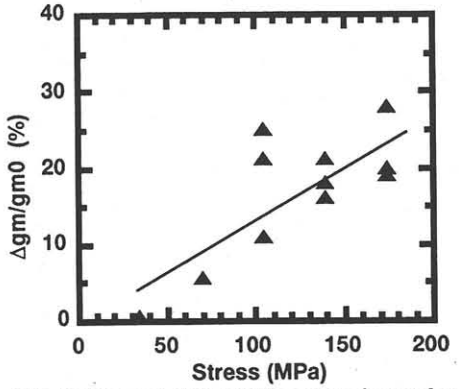

Fig. 2 The gm degradation rate dependence on the stress induced by the die-attach process.

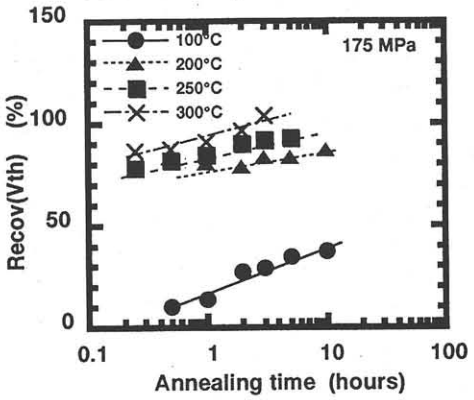

Fig. 6 The V_{th} recovery rate as a function of annealing temperature.

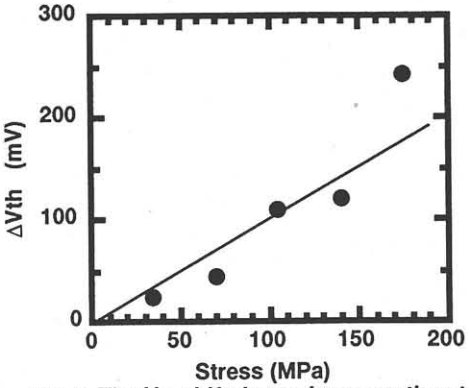

Fig. 3 The V_{th} shift dependence on the stress induced by the die-attach process.

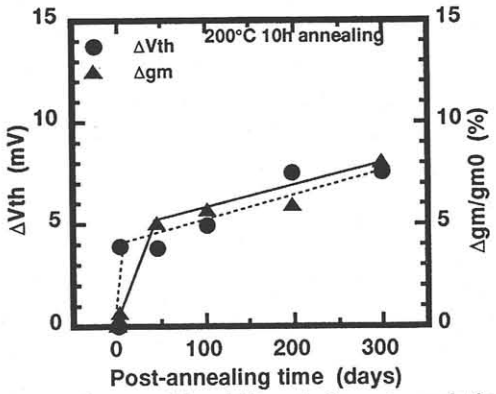

Fig. 7 Dependence of V_{th} shift and of gm degradation rate on monitor time after annealing.

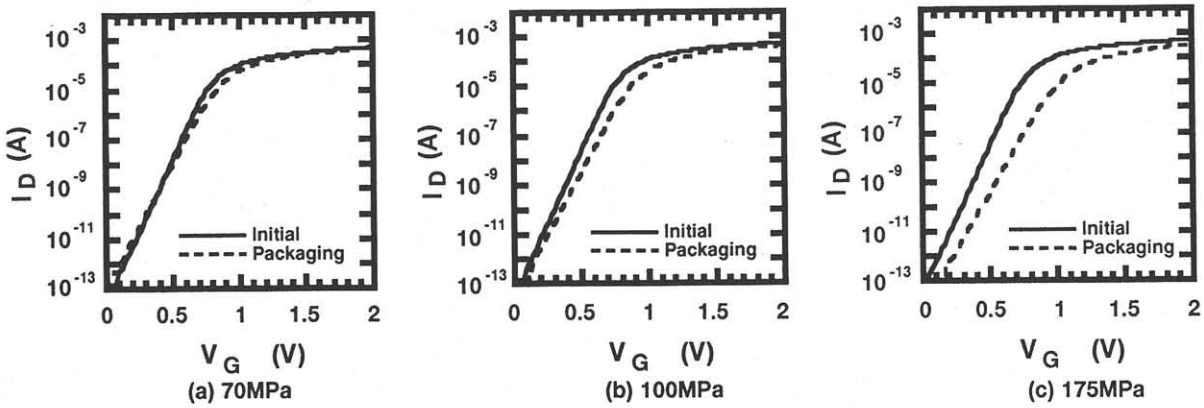

Fig. 5 Changes in I_D vs. V_G after packaging with the stress as a parameter.