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Enhanced-Mobility Deep Submicron Strained-Si n-MOSFETs

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1. Introduction

We report the first measurements of enhanced electron mobility in surface-channel, strained-Si *n*-MOSFETs with doping profiles suitable for the deep submicron regime. It has been shown that scaling of Si *n*-MOSFETs leads to lower channel mobility, which has a significant effect on device transconductance, even for deep submicron devices [1]. Hence, it is important to investigate structures which promise higher mobility. Record electron mobilities have been reported for strained-Si modulation-doped structures [2]. Electron mobility enhancement due to strain-induced conduction band splitting has previously been characterized in *n*-MOSFETs employing pseudomorphic strained Si channels grown on relaxed $Si_{1-x}Ge_x$, with low (2×10^{16} cm^{-3}) doping [3]. In this work, we present the first measurements of the mobility enhancement in strained Si *n*-MOSFETs at vertical effective fields (~1 MV/cm) typical of scaled Si devices. Even for high substrate doping, the peak electron mobilty is enhanced by ~1.75×, which is comparable to the improvement observed in lightly-doped strained Si devices at lower vertical effective fields [3]. The transconductance enhancement persists down to the shortest channel lengths studied, approximately 0.2 μm.

2. Device Fabrication

Relaxed $Si_{0.8}Ge_{0.2}$ and strained Si epitaxial layers were grown at 750°C by chemical vapor deposition. Epitaxial layer structures (Fig. 1) were designed such that after device processing, the doping profiles below the gate were comparable for the (a) strained Si/relaxed $Si_{0.8}Ge_{0.2}$ and (b) unstrained Si control (referred to as "epi Si control") devices. Boron *in-situ* doping was used to create very abrupt, p^+ (10^{18} cm^{-3}) punch-through-stoppers below the surface channel layers for both types of wafers. The slower diffusion of B in $Si_{1-x}Ge_x$ has been characterized [4], and thin *i*-$Si_{0.8}Ge_{0.2}$ boron diffusion barriers were positioned on either side of the p^+ layer, to reduce B up-diffusion into the channel layer and maintain an abrupt doping profile after device processing. *n*-MOSFETs with CVD-oxide isolation and *in-situ* n^+ polysilicon gates were fabricated using e-beam, direct write patterning for gate definition, and optical lithography for all other levels. The 67 Å-thick gate oxide was grown at 800°C by thermal oxidation of the top Si layers. CVD-oxide spacers were used, along with a Ti salicide process. Aside from the gate oxidation, the high-temperature steps include RTA of the As^+ implanted source/drains (650°C-2 min. & 850°C-15 sec.), and 650°C-2 min. for the Ti reaction step. Strain in the channel layer was measured by Raman scattering. Comparison of the measured Si-Si line shift to theoretical prediction confirms the absence of strain relaxation in the Si layers during processing.

3. Electrical Characterization

Fig. 2 shows the output characteristics for a strained Si *n*-MOSFET with drawn gate length of 0.2 μm. Fig. 3 compares the sub-threshold characteristics for strained Si and epi Si control devices. Large area devices were used to extract the effective electron mobility ($\mu_{eff}=g_D\ (L/W)/Q_{inv}$) as a function of the vertical effective field, E_{eff} [5]. The inversion charge, Q_{inv} was determined by the split-*C-V* technique [6]. Fig. 4 shows the extracted electron mobility for both types of devices, compared to the universal mobility [5]. The peak μ_{eff} is enhanced by roughly 1.75× for the strained Si compared to the epi Si control device. The enhancement persists to the highest E_{eff} measured (~1 MV/cm), suggesting that surface roughness scattering does not significantly degrade the strain-induced mobility enhancement for short-channel designs.

The shift and ratio method [7] was used to extract the effective channel lengths and series resistance. The magnitude of the ΔL correction was ~ 100 Å for channel lengths in the range of 0.2 to 0.4 μm. The source/drain series resistances, R_{SD}, are 1300 and 900 Ω-μm for the strained Si and epi Si control devices, respectively, with less than 10% variation for devices of different mask lengths. Fig. 5 compares the extrinsic g_m for the strained Si and epi Si control devices for drawn gate lengths of 0.2 μm. Due to the strain-induced mobility enhancement, g_m increases more rapidly as a function of V_{GS} for the strained Si device. The measured maximum g_m is enhanced by 25% for V_{DS} of 0.5 V.

4. Conclusions

The enhanced electron mobilities observed for high doping and vertical effective fields indicate that strain can be used to form high mobility channels for deep submicron devices, and to recover some of the degradation associated with high channel doping as devices are scaled. The peak effective mobility of 575 $cm^2/V\bullet sec$ achieved in the strained Si *n*-MOSFETs is 75% higher than the state of the art MOSFET mobility at comparable doping and effective field. Electrical characteristics of these short-channel strained Si *n*-MOSFETs are encouraging for deep submicron devices.

Acknowledgments

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References

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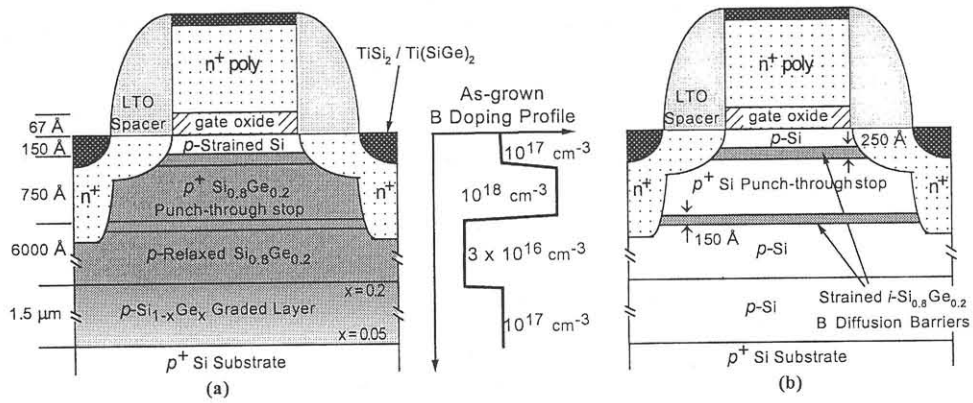

Fig. 1. Epitaxial layer structures for *n*-MOSFETs fabricated on (a) strained Si / relaxed $Si_{0.8}Ge_{0.2}$ and (b) unstrained Si control ("epi Si control"). *In-situ* doped boron profile and thin *i*-$Si_{0.8}Ge_{0.2}$ boron diffusion barriers were designed such that the doping profiles below the gate were well matched for the two structures after device processing.

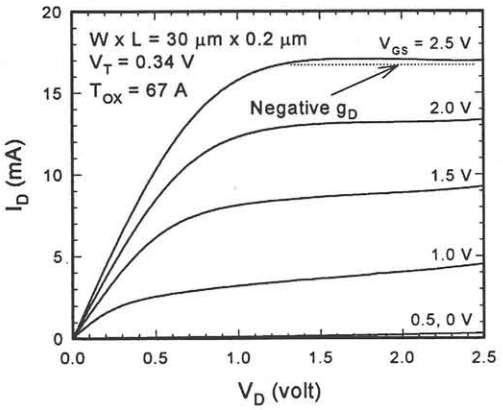

Fig. 2. Output characteristics of a 30×0.2µm² strained-Si *n*-MOSFET. At high V_{DS} and V_{GS}, negative output conductance is observed. This is caused by self-heating due to the thermal resistance of the thick, relaxed $Si_{0.8}Ge_{0.2}$ layer [8].

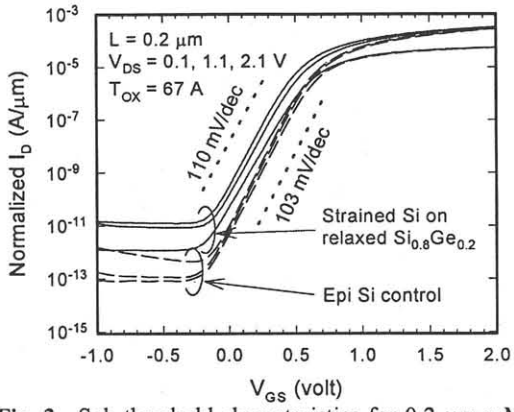

Fig. 3. Sub-threshold characteristics for 0.2 µm *n*-MOSFETs. The sub-threshold slopes are as expected for these doping profiles and T_{ox} = 67 Å. The lower conduction band energy in Strained Si reduces the threshold voltage with respect to the epi Si control devices.

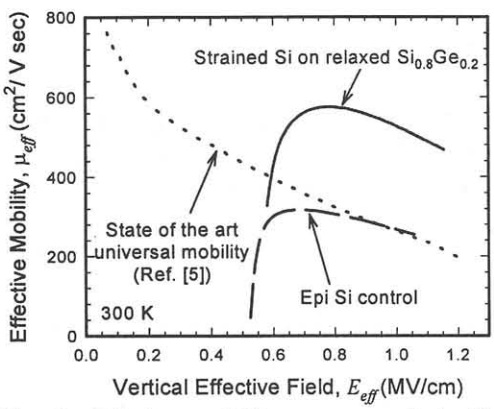

Fig. 4. Effective mobility, μ_{eff} vs. vertical effective field, E_{eff}. Even in high E_{eff} regime, mobility enhancement of over 70% is observed for strained Si/relaxed $Si_{0.8}Ge_{0.2}$ *n*-MOSFETs with high substrate doping suitable for deep submicron devices.

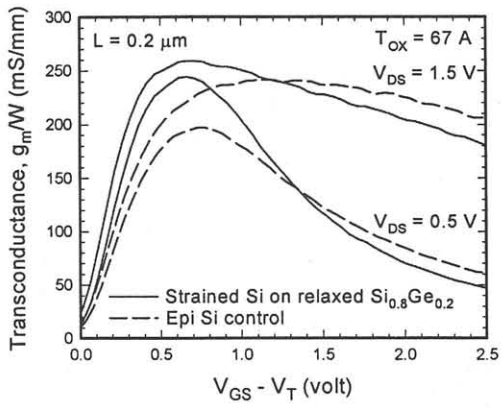

Fig. 5. 0.2 µm *n*-MOSFET transconductance, g_m. Due to the strain-induced mobility enhancement, g_m increases more rapidly as a function of V_{GS} for the strained Si device. Enhancement of the peak g_m is reduced at higher biases due to SOI-like self-heating in these strained-Si devices.