Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 94-95

Performance Considerations in Using High-k Dielectrics for Deep Sub-Micron MOSFETs

A. Inani, V. Ramgopal Rao, B. Cheng, M. Cao*, P. V. Voorde*, W. Greene*, and J.C.S. Woo
EE Department, University of California, Los Angeles, CA 90095-1594, USA
* ULSI Research Laboratory, Hewlett-Packard Laboratories, Palo Alto, CA 94304, USA

1. Introduction

With continuous shrinking of MOSFET critical dimensions, short channel effects such as DIBL and sub-threshold leakage are expected to impose a severe limit on MOSFET performance. To alleviate this problem gate oxide thickness needs to be scaled down to below 1.5 nm for a sub 0.1 μm channel MOSFET in order to meet acceptable sub-threshold leakage and DIBL criteria. It is unlikely that SiO_2 can be pushed much below 1.5 nm thickness regime because of the reproducibility and manufacturability issues and high tunneling gate leakage currents. Much effort is therefore currently underway on alternative high-K gate dielectrics such as Si_3N_4, Ta_2O_3, TiO_2 and $(Ba,Sr)TiO_3$ with the effort mainly concentrated on material issues such as achieving a stable interface with silicon as well as the gate contact material at any subsequent processing temperature. However, no detailed analysis of the effect of high-K dielectrics on sub-micron MOSFET performance has so far been undertaken and this work therefore aims at presenting detailed 2-D device simulation results in this direction.

2. Simulations

In this work we report results of gate stack architecture analysis using advanced 2-D device simulations and analyze the effect of gate fringing fields on sub-micron MOSFET performance. MOSFETs with channel lengths varying from 0.07 to 0.25 μm are studied using quantum models and energy balance models, as supported by ATLAS [1], with various gate stack architectures. An effective gate oxide thickness of 1.5 nm is used for all the simulations which is realized using (i) full high-K dielectric (ii) gate stack with a combination of 1 nm conventional oxide and a high-k dielectric and (iii) a conventional oxide. The different gate stack configurations are schematically shown in Figure 1. The K-values have been varied over a wide range from 3.9 (of SiO_2) to 200 (typical for BST) and the MOSFET performance is analyzed for short-channel effects and device performance.

3. Results and Discussion

Figure 2 (a) shows the V_T shift with increasing dielectric constant for T_{ox} (eff)=1.5 nm and L=0.07 μm. It can be noticed that the stack structure shows much lower V_T shift with increasing K-value compared to the full high-K MOSFETs. In Figure 2 (b) are shown the sub-threshold slope (S) and DIBL as a function of K for a 0.07 μm channel length MOSFET using a 1.5 nm effective gate oxide thickness. As can be seen, a higher K value results in degraded short-channel performance counteracting the effect of oxide thickness scaling in this regime. In Figure 3 the effect of channel length on short-channel effects is plotted with different gate stack combinations. With increasing K-value, and for the same T_{ox} (eff)=1.5 nm, the physical thickness (T_k) to the channel length (L) ratio increases. As can be seen from Figs. 2 and 3, it is apparent that maintaining a lower T_k/L value is desirable to achieving a tolerable DIBL and sub-threshold slopes in short-channel MOSFETs. The degradation in MOSFET performance with increasing K-value is analyzed using 2-D device simulations. Figure 4 shows the effect of device fringing field for a full high-K and a conventional oxide MOSFET [2]. As can be noticed, increasing physical gate oxide thickness (i.e., increasing K) results in higher gate fringing field which reduces the gate control in sub-micron MOSFETs. This degrades the short-channel effects as well as the MOSFET threshold voltage at higher T_k/L values. For a less than 20% degradation in DIBL with respect to conventional gate oxide MOSFETs, the T_k/L value must be maintained below 0.15 as observed from our detailed simulations as a function of channel length and physical gate oxide thickness.

4. Conclusions

Sub-micron MOSFET performance with different gate stack architectures is analyzed. It has been shown that increasing T_K/L value degrades the MOSFET short-channel performance due to the effect of fringing field. T_k/L value above 0.15 degrades the DIBL by more than 20 % compared to a conventional MOSFET.

References

1. ATLAS, SILVACO tools, Santa Clara, CA
2. B. Cheng *et al.*, to be presented at ESSDERC '98, Bordeaux, France.

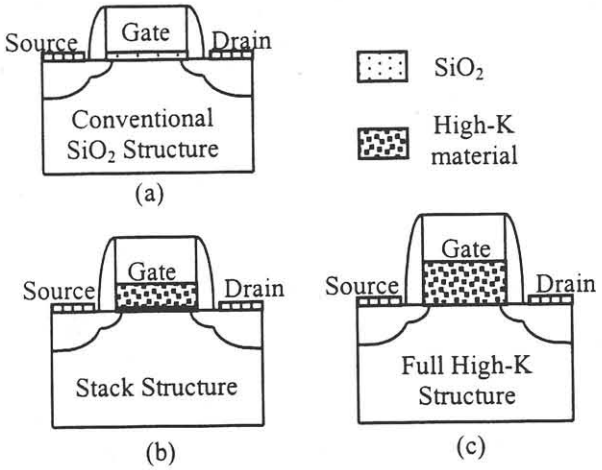

Figure 1 : Various MOSFET structures used for simulations. MOSFET with (a) conventional SiO_2 dielectric (b) Gate stack with a 1 nm oxide and high-K (c) Full high-K dielctric. Effective oxide thickness is kept at 1.5 nm for all the cases.

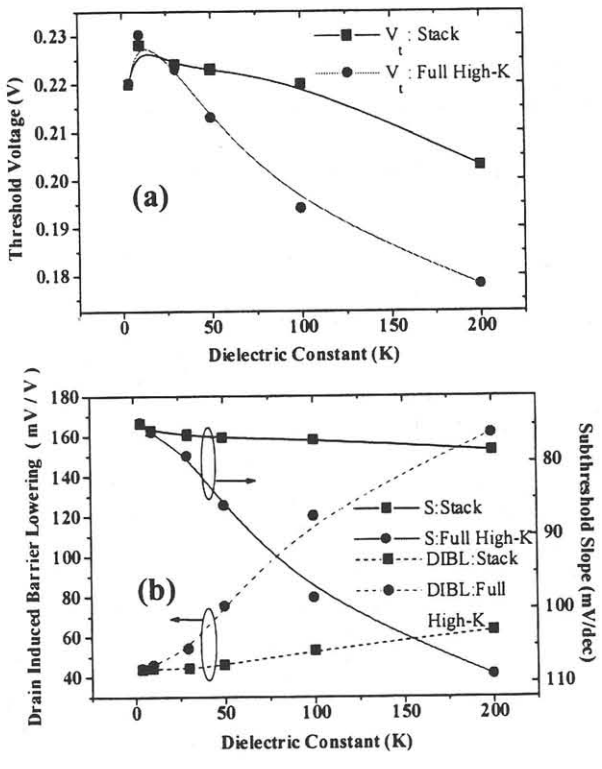

Figure 2 : Variation in (a) threshold voltage and (b) DIBL and sub-threshold slopes as a function of dielectric constant. The T_{ox} (eff) =1.5 nm in all the cases and channel length is 0.07 μm. Full high-K structure is simulated with K=200 and the stack structure consists of a high-K with K=200 and a conventional oxide with K=3.9.

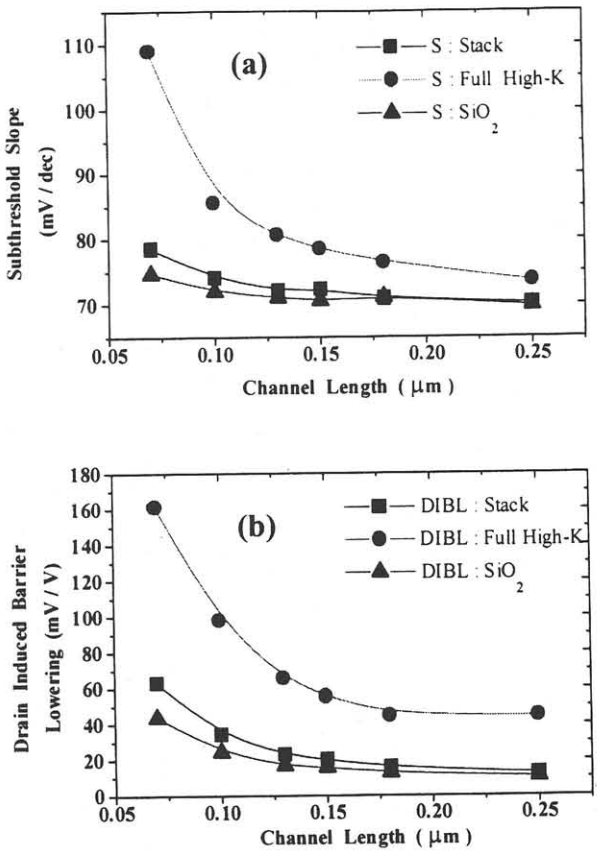

Figure 3 : Variation in (a) sub-threshold slope, S and (b) DIBL as a function of channel length. T_{ox} (eff) =1.5 nm in all the cases. Full high-K structure is simulated with K=200 and the stack structure consists of a high-K with K=200 and a conventional oxide with K=3.9 .

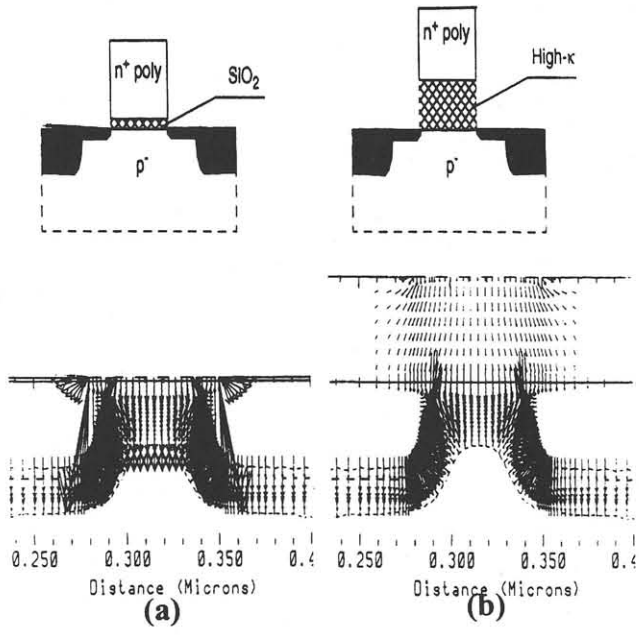

Figure 4 : Fringing field distribution for a 0.07 μm channel length MOSFET with (a) Conventional gate oxide and (b) Full high-K dielectric.