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A Fatigue-Tolerant MFOS Structure with Large Memory Window of 3.6V Using Sr-Deficient and Bi-Excess SBTO Ferroelectric Film Prepared on SiO_2/Si at Low Temperature by PLD Method

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1. Introduction

In recent years ferroelectric memory devices have attracted much attention from the viewpoint of the next generation of highly integrated circuits. DRAM is volatile memory, and so it is desired that nonvolatile memory should be developed. There are mainly two kinds of nonvolatile memories using ferroelectric thin films. One is FET using ferroelectric storage capacitor having large D-E hysteresis. The other is Metal-Ferroelectric-(Insulator)-Semiconductor FET (MF(I)SFET) which has ferroelectric thin film gate. Especially, the latter FET is superior among the memory devices as the memory is read out nondestructively.

We have concentrated on investigating Metal-Ferroelectric-Oxide-Semiconductor (MFOS) structure. The oxide is SiO_2 because Si-SiO_2 combination is believed to be the most stable and promising I-S structure, in order to control precisely gate potential on FET channel due to excellent I-S interface characteristics and also to get reliabilities including fatigue or retention characteristics in the MFIS FET operation. It is considered that charge injection phenomena tend to occur in the insulator film deteriorated during the ferroelectric film deposition at high temperature and degrade dielectric hysteresis mode, that is, memory window characteristics. Therefore, we have primarily proceeded to get a low leakage MFOS diode structure.

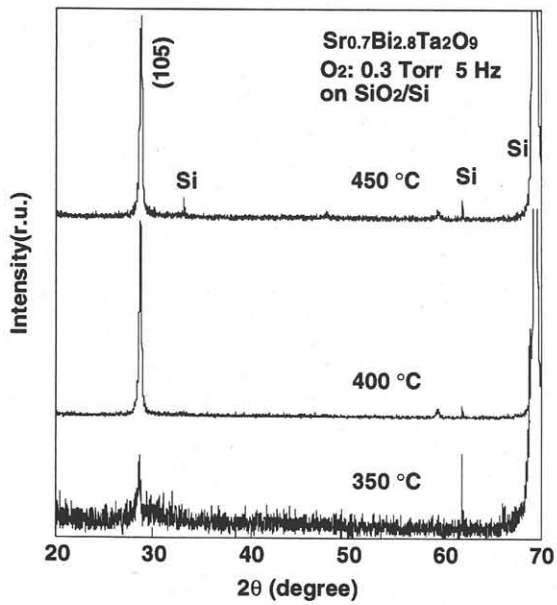

Fig.1 XRD patterns of $Sr_{0.7}Bi_{2.8}Ta_2O_9$ films on SiO_2/Si wafers as a function of substrate temperature

2. Experimental Results and Discussions

In this work, $Sr_xBi_{2+y}Ta_2O_9$ with thickness of about 500 nm has been prepared by Pulsed Laser Deposition (PLD) method, and thermal oxide SiO_2 with thickness of about 40 nm were used as the oxide layers on an n-Si substrate with resistivity of about 50Ωcm. Sharp (105) peaks are observed for every substrate temperature (T_s), especially even for a low temperature of 350°C as seen in Fig.1. And therefore preferentially (105)-oriented perovskite structure is recognized. Note that our XRD patterns of SBTO films on SiO_2/

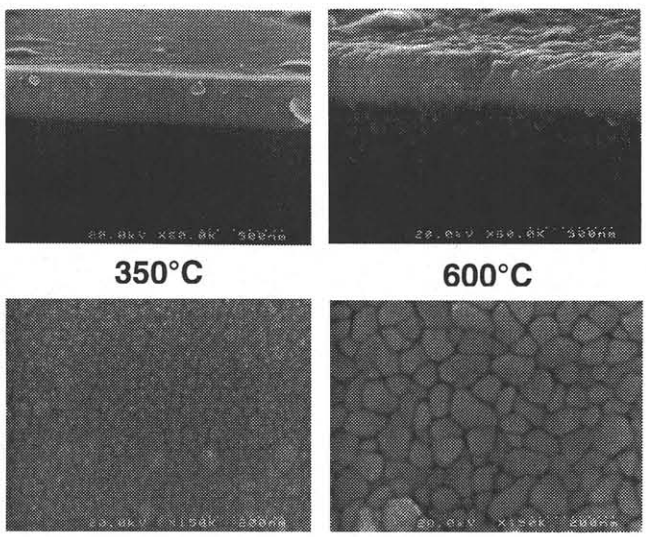

Fig.2 Cross-sectional and surface views of $Sr_{0.7}Bi_{2.8}Ta_2O_9$ on SiO_2/n-Si(100) diode structure as a parameter of substrate temperature

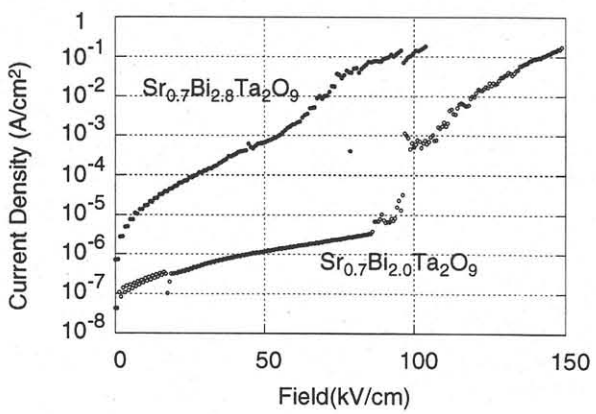

Fig.3 Current density vs. electric field for Al/$Sr_{0.7}Bi_{2+x}Ta_2O_9$/SiO_2/n-Si(100) diode structure when forward biased as a parameter of x (=0.8,0) in laser ablation deposition

Si wafers also show preferentially (105)-oriented perovskite structure even when Sr/Bi composition is changed. Leakage current through MFOS structure became reduced successfully by more than 2 orders by lowering its growth temperature, which induces suppression of the leakage due to decrease in grain size and various interface reactions in an MFOS structure as seen from Fig.2. This leakage current is also reduced by changing Sr/Bi composition to Sr deficient and Bi excess, as shown in Fig.3. This reduction should be related to the fact that composition variation around the stoichiometric 1/2/2 composition was much related to grain size, which grows larger in stoichiometric composition than in Sr-deficient and Bi-excess composition [1]. Therefore, these improvements in the leakage reduction may be related to decreased grain size of SBTO thin film, and/or by suppressing interdiffusion between F-I-S interfaces,.

Then we have focussed on evaluating memory window, which is a key factor for realizing a practical memory FET, from the viewpoint of leakage, that is, growth temperature and Sr/Bi composition. Memory window is increased with decreasing the temperature from 600 to 350°C (Fig.4), and also with decreasing Bi composition from 2.8 to 2.0 when Sr composition of 0.7 (Fig.5). Memory window of as large as

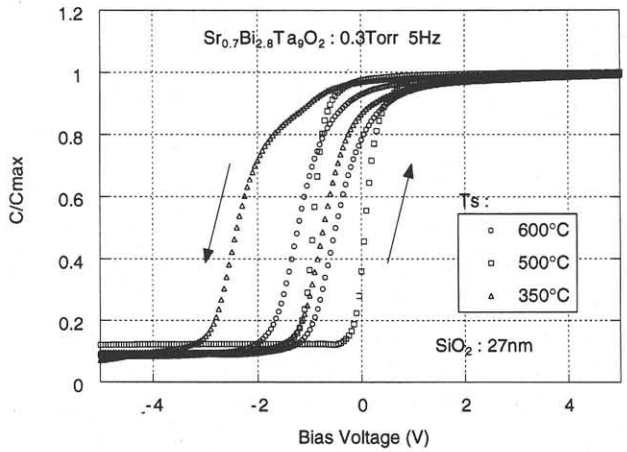

Fig.4 C-V characteristics of Al/$Sr_{0.7}Bi_{2.8}Ta_2O_9$/SiO_2/n-Si(100) diode structure as a function of substrate temperature in laser ablation deposition (measured frequency: 1MHz)

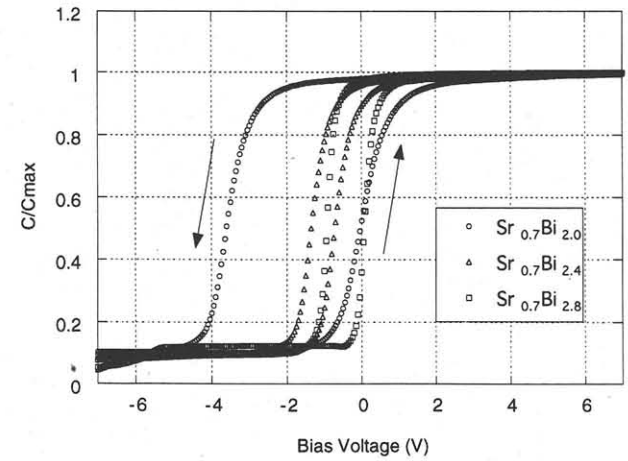

Fig.5 C-V characteristics of Al/$Sr_{0.7}Bi_{2+x}Ta_2O_9$/SiO_2/n-Si(100) diode structure as a function of x (=0.8,0.4,0) in laser ablation deposition (measured frequency: 1MHz)

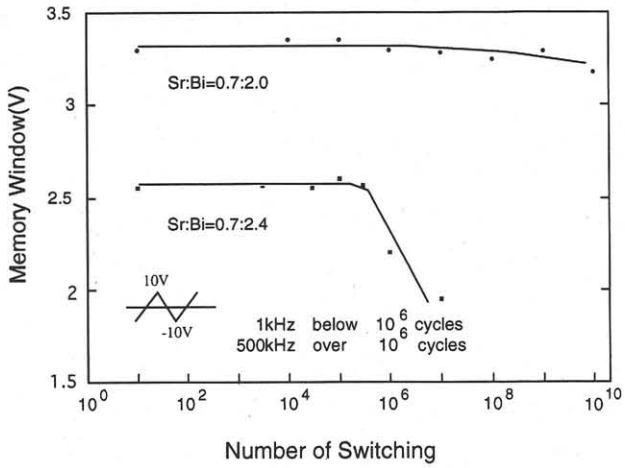

Fig.6 Fatigue characterisics of memory window in C-V curve in MFIS diode structure for Sr/Bi of 0.7/2.0 and 0.7/2.4

3.6V has been obtained in the MFOS capacitor when Sr/Bi composition is 0.7/2.0, to our best knowledge, which is the largest value in those of ever reported MFIS diode structures.

Next, fatigue characteristics were evaluated with an MFOS capacitor itself not with MFM one, since ferroelectric thin film characteristics depend strongly on the kind of growth substrate. Figure 6 indicates that little fatigue degradation is observed for Sr/Bi of 0.7/2.0 up to fatigue cycle over $1x10^{10}$, keeping memory window of more than 3.2V. For Sr/Bi of 0.7/2.4, on the other hand, the degradation starts to occur for more than 1e6.

3. Conclusions

We have prepared a preferentially (105)-oriented $Sr_{0.7}Bi_{2.8}Ta_2O_9$ thin film on SiO_2/n-Si(100) by laser ablation at low temperature as low as 350°C, which is the lowest process temperature for growing a SBTO ferroelectric thin film. Dielectric properties of the SBTO film have been improved by changing Sr/Bi atomic ratio from 0.7/2.8 to 0.7/2.0. At the Bi ratio of 2.0, a memory window of as large as 3.6V in the MFIS capacitor has been obtained and is the largest value in those of ever reported MF(I)S diode structures. Also little C-V degradation is observed for Sr/Bi of 0.7/2.0 up to fatigue cycle over $1x10^{10}$, keeping memory window of more than 3.2V.

Finally, we should make a special emphasis on that improvement in memory characteristics is strongly related to insulating properties of MFIS diode structure. It is concluded that a low temperature process in preparing ferroelectric thin film and Sr-deficient and Bi-excess SBTO thin film by PLD method are very effective and promising for realizing an excellent MFI(O)S FET structure.

Reference

[1] T. Noguchi et al: Jpn. J. Appl. Phys. **35** (1996) 4900.

Acknowledgments

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