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Preparation of $Bi_4Ti_3O_{12}$ Thin Films by MOCVD Method and Electrical Properties of MFIS Structure

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1.Introduction

Since MFS-FET (Metal/Ferroelectric/Semiconductor Field Effect Transistor) was first reported by Moll and Tarui [1], its application for nonvolatile ferroelectric memories device with nondestructive readout operation has been expected. In MFS structure, it is difficult to obtain the good ferroelectric thin films directly deposited on Si substrate because of the interface reaction between ferroelectric materials and the Si substrate, such as the generation of mobile ions and low retention. Recently, MFIS structure (metal/ferroelectric/insulator/semiconductor) was extensively investigated in order to avoid such an interface reaction. In this study, we propose a new material of Bi_2SiO_5 for insulator layer of MFIS structure with ferroelectric $Bi_4Ti_3O_{12}$ thin film. It was succeeded that a smooth surface of c-axis oriented $Bi_4Ti_3O_{12}$ thin film with good ferroelectric properties was obtained on Si(100) substrate using Bi_2SiO_5 intermediate buffer layer by low temperature MOCVD method.[2]

2.Experimental

Bi_2SiO_5 and $Bi_4Ti_3O_{12}$ thin films were deposited on Si(100) single crystal substrates by the same MOCVD method we previously reported.[2] Its deposition conditions is shown in Table 1. In order to form Bi_2SiO_5 buffer layer on p-Si(100) substrates, Bi source and O_2 oxidation gases were supplied for 30 minutes at 500℃ without Ti source. In this way, the native oxide layer on Si surface was removed before the film deposition. Next, $Bi_4Ti_3O_{12}$ film was deposited on the Bi_2SiO_5 layer using Bi, Ti source and O_2 gases at 500℃. The crystalline structure and the surface morphology of films were characterized by X-ray diffraction (XRD) analysis and scanning electron microscopy (SEM). To fabricate the MIS and the MFIS structures, Pt top electrode and Al bottom electrode was deposited by the evaporation method at the room temperature. The C-V characteristics and the retention time measurements were carried out at 1MHz with an LCR meter (4275A, Yokogawa Hewlett-Packard). The leakage current density and the D-E hysteresis loops when the Si surface was used as the bottom electrode were measured using a pA meter connected to a DC voltage source and a RT66A ferroelectric test system (Radiant Technologies, Inc) with a frequency of 1kHz.

Table I Deposition conditions

Precursors	$Bi(o\text{-}C_7H_7)_3$	$Ti(i\text{-}OC_3H_7)_4$
Precursors temp.	160℃	50℃
Gas flow rate		
Ar carrier gas	250sccm	50sccm
O_2 gas	1000sccm	
Total gas flow rate	2500sccm	
Pressure	2-10Torr	
Substrate	p-Si(100)	

3.Results and Discussion

Figure 1 shows the XRD patterns of Bi_2SiO_5/Si and $Bi_4Ti_3O_{12}/Bi_2SiO_5$/Si structure where the a-axis oriented Bi_2SiO_5 film on Si(100) substrate and c-axis oriented $Bi_4Ti_3O_{12}$ film on Bi_2SiO_5 layer were observed. Then, the SEM image of Bi_2SiO_5/Si and $Bi_4Ti_3O_{12}/Bi_2SiO_5$/Si structure shows separated layers and flat and smooth surface morphology(Fig.2). We therefore suggest that the surface region of Si substrate was transformed to Bi_2SiO_5 crystalline film. A similar preparation method of bithmuth silicate films was also reported by Kims.[3]

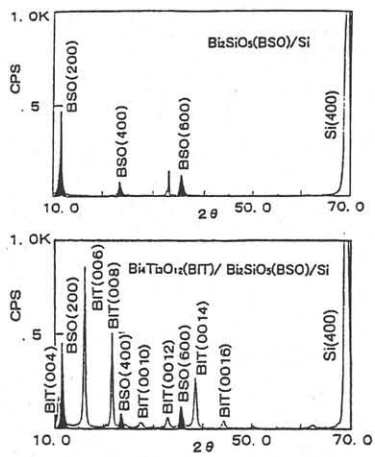

Fig.1 XRD patterns of Bi_2SiO_5/Si and $Bi_4Ti_3O_{12}/Bi_2SiO_5$/Si.

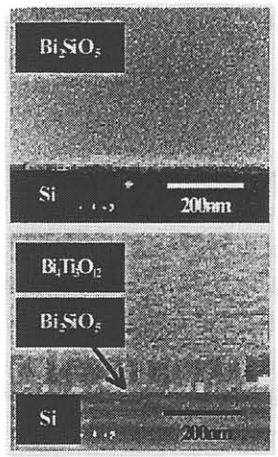

Fig.2 Surface morphorogies of Bi_2SiO_5/Si and $Bi_4Ti_3O_{12}/Bi_2SiO_5$/Si.

Figure 3 and 4 shows the C-V characteristics of Pt/Bi_2SiO_5/Si/Al and Pt/$Bi_4Ti_3O_{12}/Bi_2SiO_5$/Si/Al. The film thickness of Bi_2SiO_5 was 30nm and that of $Bi_4Ti_3O_{12}$ were 100, 200 and 400nm.

Bi_2SiO_5 film showed well defined C-V characteristics, i.e. no C-V hysteresis properties was observed. The dielectric constant estimated from the capacitance value was about 30.

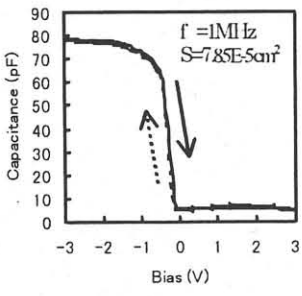

Fig.3 C-V characteristics of Pt/ 30nmBi_2SiO_5/Si/Al.

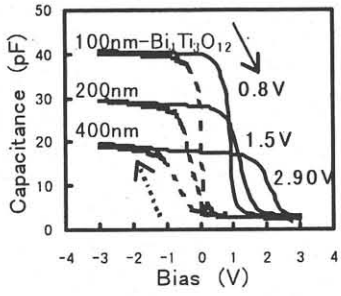

Fig.4 C-V characteristics of Pt/ $Bi_4Ti_3O_{12}$/30nmBi_2SiO_5/Si/Al.

On the other hand, $Bi_4Ti_3O_{12}$ films showed C-V hysteresis properties and these memory windows of each MFIS structure were almost proportional to $Bi_4Ti_3O_{12}$ film thickness (0.8V, 1.5V and 2.9V for 100, 200 and 400nm films, respectively). Thus the dielectric constants were estimated for each films. These were 138, 144, and 161 for 100, 200 and 400nm films, respectively. Since, D-E hysteresis loops of all films were observed at the same time, it is confirmed that these C-V hysteresis properties were due to the ferroelectrocity of $Bi_4Ti_3O_{12}$ films. In this time, memory windows were in proportion to coercive voltages. As an example, the D-E hysteresis loops of the 100nm $Bi_4Ti_3O_{12}$ film on Si substrate was shown in Fig5. When the applied voltage varied from ±1.5 to ±5V, the memory windows changed from 0.2 to 0.8V(Fig.6).

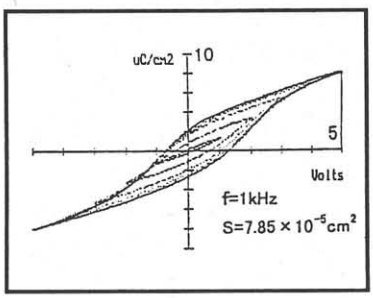

Fig.5 D-E hysteresis loops of non-annealed 100nm-$Bi_4Ti_3O_{12}$.

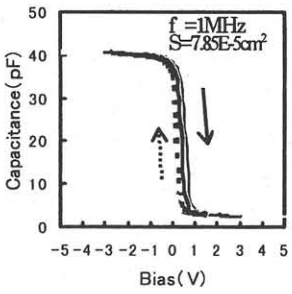

Fig.6 C-V characteristics of non-annealed 100nm-$Bi_4Ti_3O_{12}$.

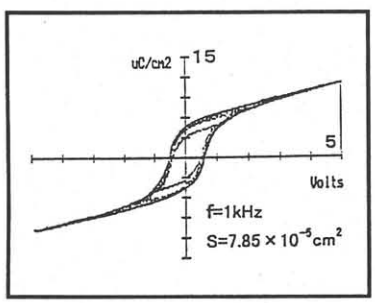

Fig.7 D-E hysteresis loops of annealed 100nm-$Bi_4Ti_3O_{12}$.

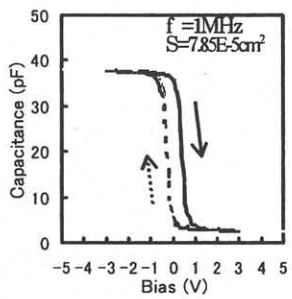

Fig.8 C-V characteristics of annealed 100nm-$Bi_4Ti_3O_{12}$.

Next, we annealed this sample at 800°C for 2 hours in the air, then the D-E hysteresis loops were saturated except for 1V(Fig.7). In this time, memory windows as shown in Fig.8 were saturated about 0.7V more than ±1.5V with the influence of the good saturation characteristics of D-E hysteresis loops. It suggests that the interface of our MFIS structure keeps good condition even after the annealing of 800°C and the value of the memory window doesn't almost change. These results show that the annealed our new MFIS structure can read and write by the low voltage of 1.5V.

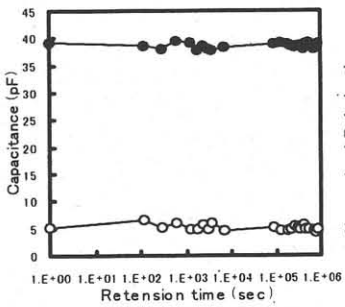

Fig.9 Retention property of Pt/100nm-$Bi_4Ti_3O_{12}$/30nmBi_2SiO_5/Si/Al.

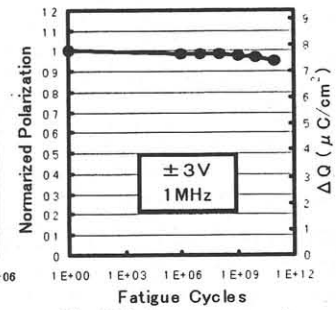

Fig.10 Fatigue property of 100nm-$Bi_4Ti_3O_{12}$.

The retention properties of annealed MFIS structure (100nm-$Bi_4Ti_3O_{12}$) was also examined at the room temperature. After the write bias voltage of +3V or –3V was applied to the sample, the time dependence of the capacitance was measured at zero-bias and it was almost constant for 11 days as shown in Fig.9. Finally, when the important fatigue property was measured for the memory devices, the degrades of the switching charge (ΔQ) was very scarce about 4% as shown in Fig10 through enduranee cycling of 10^{11} at 3V.

All these results demonstrate that our new bismuth silicate intermediate buffer film is very effective to fabricate high-quality ferroelectric thin films on Si substrate for MFIS structure at low temperature.

4.Conclusions

The Pt/$Bi_4Ti_3O_{12}$(001)/Bi_2SiO_5(100)/Si(100) substrate structure was fabricated by using the MOCVD method at 500°C. Bi_2SiO_5 film is very useful for the insulator of MFIS structure, because of the relative high dielectric constant (ε_r=30). The memory window in C-V characteristic is about 0.8V and the retention time estimated by the zero-bias capacitence is almost constant for more than 11 days at the Pt/100nm-$Bi_4Ti_3O_{12}$/30nm-Bi_2SiO_5/Si substrate/Al structure.

References

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