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Proposal of a Novel Ferroelectric-Gate Field Effect Transistor with Separated Functions for Data read-Out and Data Storage

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1. Introduction

Recently, studies on MFSFETs (metal-ferroelectric-semiconductor field effect transistors) and related devices have become important and in these devices a dielectric buffer layers is often inserted between the ferroelectric gate material and Si substrate in order to obtain good interfacial electrical properties between them. However, in the gate structure with MFIS (I : insulator) or MFMIS layers, a series connection of ferroelectric and dielectric capacitors is included and depolarization field is inevitably generated in the ferroelectric film, when the gate electrode is grounded. This depolarization field is considered to be a main factor to shorten the retention time of FET-type ferroelectric memories. In this paper, I propose a novel ferroelectric-gate FET in which the depolarization field is not generated in the ferroelectric film, even if the gate electrode is grounded.

2. Structure and Write Operation

An equivalent circuit of the FET is shown in Fig.1, in which two ferroelectric capacitors are connected to the gate of a usual MOSFET with a SiO_2/Si interface, forming a floating gate structure. It is assumed that the material and size of the capacitors are the same and only their thicknesses are different. In order to write "0" or "1" datum in this memory, positive or negative voltage is applied between the terminals A and B. In this paper, the data "0" and "1" are defined as shown in Figs.1 (a) and (b), respectively. In this structure, the MOS gate capacitor C_{OX} is necessary to be relatively small, since the floating gate potential is virtually grounded for very large C_{OX} and the voltage difference between the floating gate and the terminal A or B is not large enough to saturate the polarization of the ferroelectric film. If the substrate potential of MOSFET is appropriately biased during the write operation, the restriction for C_{OX} is unnecessary to be taken into account.

When both ferroelectric capacitors reach the saturation polarization, equal amount of positive and negative charges appears on the electrodes of the capacitors C_A and C_B, and thus no charge appears on the electrode of capacitor C_{OX}. Under this condition, the floating gate potential which is given by $V_{OX} = Q_{OX} / C_{OX}$ is zero and no depolarization field is generated for both C_A and C_B, when the terminals A and B are grounded. It is evident that the retention time of this memory is as long as that of the usual 1T1C type (or 2T2C type) memories, in which ferroelectric capacitors are short-circuited when the power supply is turned-off.

3. Nondestructive Read-out Operation

In order to read-out the stored data, positive pulse voltage V is applied to the terminal B, the terminal for the thinner ferroelectric film, keeping the Si substrate grounded and the terminal A open. When the stored datum is "0", no polarization reversal occurs by the read-out pulse and no electrons are induced on the Si surface, as shown in Fig.2(a). On the contrary, when the stored datum is "1", polarization of the capacitor C_B is reversed and electrons are induced on the Si surface, as shown in Fig.2(b), which means that the drain current flows in the n-channel MOSFET. After the read-out pulse is removed, that is, both terminals A and B are grounded, the polarization direction of the capacitor B is expected to be automatically aligned to that of the capacitor A, since the coercive voltage of the capacitor A is much larger than that of B. This simple model is essentially correct, if the capacitance C_{OX} is infinitely small. For a finite C_{OX}, however, a more precise discussion is necessary.

I assume an ideal Q-V hysteresis curve for the capacitor C_B, as shown in Fig.3, where Q_B and V_B are the induced charge on the electrode and the voltage across C_B, respectively. Characteristics close to the ideal ones have actually been observed recently.[1)] The charge distributions on the electrodes during the read-out operation are schematically shown in Figs.4 (a) and (b), in which (a) corresponds to the initial condition at "0" state. Three relations $V=V_B+V_{OX}$, $Q_B=Q_{BR}+Q_{OX}$ (Q_{BR}: charge induced by remnant polarization), and $Q_{OX}=C_{OX}V_{OX}$ are derived from the figure and they give an equation of the form of $Q_B=Q_{BR}+C_{OX}(V-V_B)$, which is shown in Fig.3 in solid lines. Similarly, broken lines are obtained for the initial "1" state.

It is evident from Fig.3 that the read-out pulse does not destroy "0" datum, while it change "1" state from the original position L. If the applied voltage V is large enough, the operation point moves along the outermost hysteresis loop and comes back to a new position M. The direction of electric field in the film is the same as that of polarization, as long as it is located in the third quadrant, as shown in the figure, and thus no depolarization field is generated. However, since a voltage equal to the coercive voltage is generated in the capacitor C_B and since the polarization directions of C_B and C_A are opposite in parallel connection of both capacitors, this voltage produces a depolarization field in C_A. Because of this field, the remnant polarization of C_A decreases until the remnant polarization values of both capacitors are equal. A new equilibrium is expected to be reached around the position N in Fig.3. Since the decrease of

the remnant polarization in C_A is on the order of several hours to several days, the position M is not changed drastically, even if the read-out operation is frequently repeated in a short time, and the stored data are expected to be preserved, if the rewrite (refresh) operation is conducted once in a hour or in a day. It should be noted that the depolarization field disappears when the remnant polarization of both capacitors becomes equal and that value is kept for a long time even if the power supply is turned off. This feature is completely different from a simple MFIS or MFMIS-type FET, in which the remnant polarization becomes zero due to the depolarization field.

4. Layout for High-Density Integration

In order to integrate the unit cell shown in Fig.1, I propose to use an SOI (silicon-on-insulator) structure. The structure shown in Fig.5 is a simple extension of the single-transistor-cell-type memory proposed by us.[2] In this structure, Si stripes, each of which corresponds to parallel connection of MOSFETs, are placed on an insulating substrate, floating gate electrodes are placed along the stripes on the gate SiO_2 film, and double metal (or conductive oxide) stripes embedded in a ferroelectric film are placed parallel and perpendicular to the Si stripes. The size of the floating gate and the width of the double metal stripes are so determined that the overlap area between the floating gate and the first metal stripe is equal to that between the floating gate and the second metal stripe, as shown in the inset of the figure. Thus, the capacitors C_A and C_B are formed on the floating gate without any precise mask alignment. In the write operation, the double metal stripes are used, while in the read-out operation, current between the source and drain regions in a Si stripe is measured by applying a voltage pulse to the first metal stripe. [2]

5. Summary

A novel ferroelectric-gate FET was proposed and its write and read-out operations were explained. This memory FET has the following features ; (1) no depolarization field is generated if the data are not read-out, (2) the depolarization field which is generated through the read-out operation reduces the remnant polarization only partly, if the device structure is optimally designed, and (3) the FETs can be laid-out in high-density. These features enable us to fabricate a novel virtually nondestructive-read-out-type ferroelectric memory with a long retention time, where the term 'virtually' means that the stored data are refreshed typically once a day when the device is connected to a power supply. Some preliminary simulation results have been obtained using a SPICE model of a ferroelectric capacitor. [3]

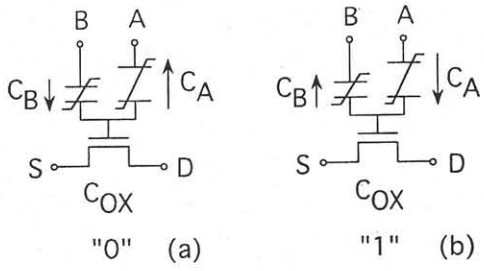

Fig. 1

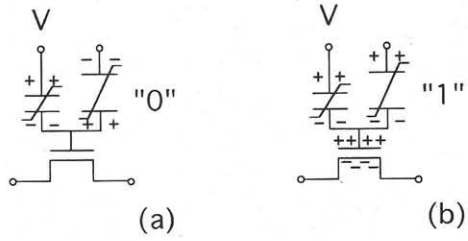

Fig. 2

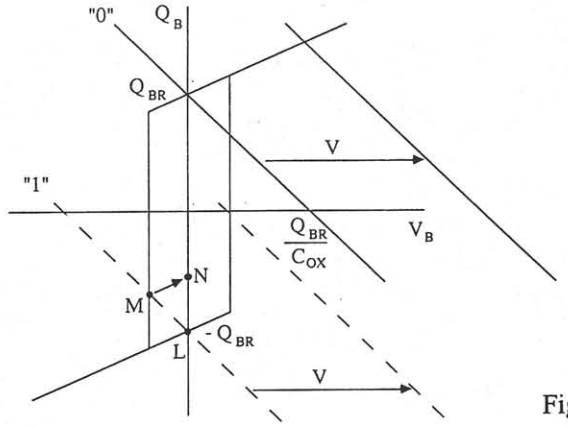

Fig. 3

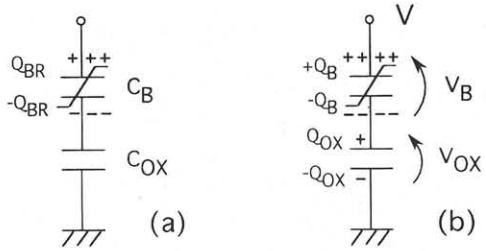

Fig. 4

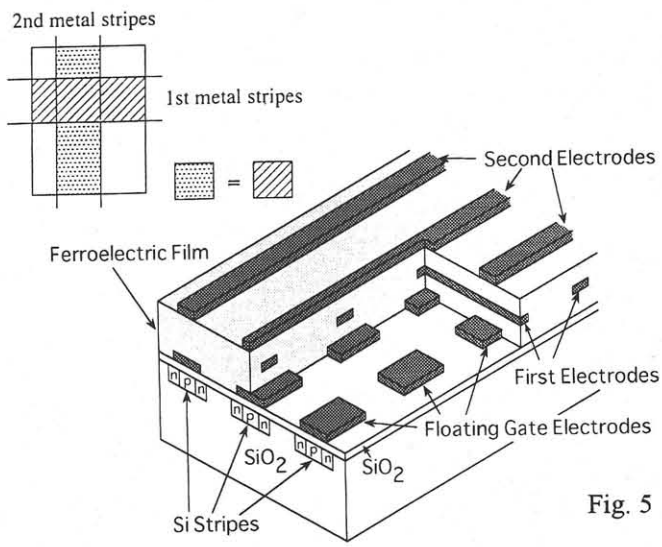

Fig. 5

Reference

1) D. J. Wouters et al : 1998 Intern. Sympo. on Integrated Ferroelectrics, No. 187C
2) H. Ishiwara et al : Jpn. J. Appl. Phys. **36** (1997) 1655
3) K. N. Lim et al : 1997 Intern. Sympo. on Integrated Ferroelectrics, No. 32P