Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 224-225

Properties of Ferroelectric Memory FET Using $Sr_2(Ta,Nb)_2O_7$ Thin Film

Yoshikazu Fujimori, Naoki Izumi, Takashi Nakamura and Akira Kamisawa
Process Technology Div.,ULSI Research and Development Headquarters, ROHM CO., LTD.
21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan
Phone: +81-75-321-4318 / Fax: +81-75-311-0643 / E-mail: fujimori@rohm.co.jp

1. Introdction

An FET type of ferroelectric memory has been focused, because it has a potential for a high density and high speed non-volatile memory. $Sr_2(Ta,Nb)_2O_7$ (STN) thin films are suitable as a ferroelectric material for ferroelectric memory FETs, because it has low dielectric constant (ϵ), low coercive field (E_c) and thermal stability[1].

In this paper, MFMIS (Metal Ferroelectric Metal Insulator Semiconductor) capacitors and FFRAM (Floating gate type Ferroelectric RAM) cells using STN thin films were prepared. We evaluated the electrical properties and the SIMS (Secondary Ion Mass Spectoroscopy) depth profiles. Retention characteristics of the MFMIS capacitor using STN thin films were firstly measured.

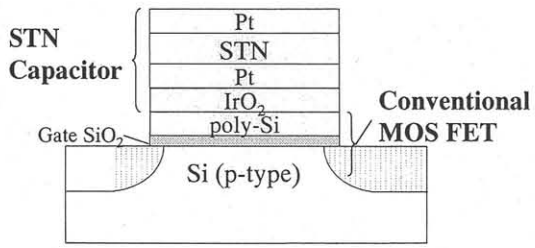

Figure 1: Schematic figure of MFMIS FET (FFRAM cell).

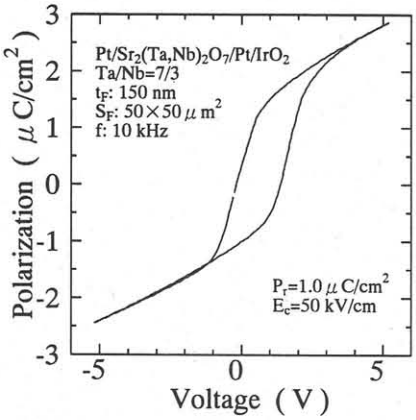

Figure 2: P–V hysteresis characteristics of STN thin film.

2. Experimental Procedure

Figure 1 shows a schematic figure of MFMIS FET using STN thin films. STN thin films were prepared on Pt/IrO_2 electrodes by the sol-gel method. The composition of the precursor was Sr:Ta:Nb=2.0:1.4:0.6. After spin coating of the STN precursor, the films were baked at 180°C for 3 min and preannealed at 400°C for 20 min in dry air. After several times of these process, these films were crystallized at 950°C in oxygen for 30 sec by RTA (Rapid thermal Annealing). Top electrodes (Pt 175 nm) were deposited on these films by sputtering and patterned by dry etching.

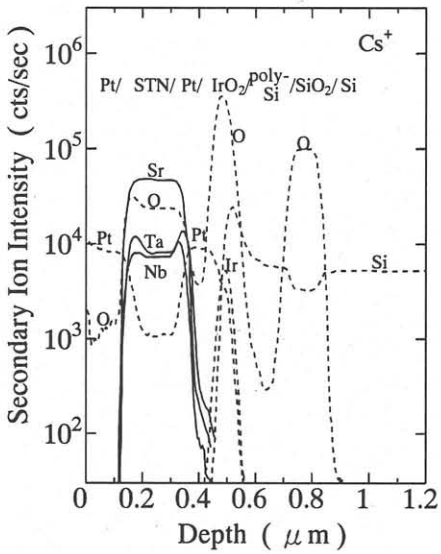

Figure 3: SIMS depth profiles of the STN capacitor.

The MFMIS capacitors were prepared for C–V measurement. The area of the STN capacitor was $50 \times 50 \mu m^2$ and the thickness of the STN and SiO_2 were 150 nm and 13 nm, respectively. 0.6μm rule FFRAM cells using the STN thin films were fabricated for I_D–V_G measurement.

Ferroelectric characteristics were measured by conventional Sawyer-Tower circuit. C–V and I_D–V_G characteristics of the FFRAM cell were measured using 4284A and 4155A (Hewlett Packard), respectively.

3. Results and Discussions

Figure 2 shows the P–V hysteresis characteristics of the STN capacitor. It exhibits a voltage shift and well saturated properties. The ferroelectric characteristics of this film are spontaneous polarization $P_r = 1.0 \mu C/cm^2$ and $E_c = 50 kV/cm$.

SIMS depth profiles were shown in Fig. 3. Metal elements in STN ferroelectric (Sr, Ta and Nb) were observed only in the ferroelectric layer. It means that the Sr, Ta and Nb never react with Pt and never diffuse into the

electrodes because of a high stability of their oxide.

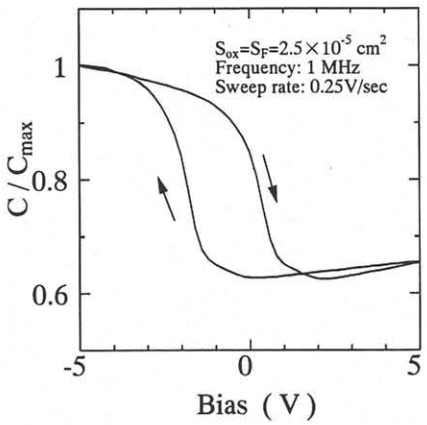

Figure 4: C–V characteristics of MFMIS capacitor using STN thin films.

Figure 4 shows C–V characteristics of MFMIS capacitor using STN. The C–V hysteresis were caused by ferroelectric polarization reversal of the STN thin films. I_D–V_G characteristics of the FFRAM cell in this study are shown in Fig. 5. The I_D–V_G hysteresis was also observed. When the applied voltage was ±5 V, memory window of 3.8 V was obtained. We succeeded to operate FFRAM cell with lower voltage than that using PZT.[2]

Figure 6 shows a data retention characteristic measured from the C–V pattern. After applying the DC bias of +5 V or −5 V, the bias voltage was changed to 0 V (short in the DC circuit). Then, the capacitance of the MFMIS capacitor was measured. The data storage and measurement temperature was 25°C.

The capacitance changed along the logarithm of the retention time. The full line in the figure was a least square fitting by the below equation.

$$C(t) = C|_{t=1} + A \ln t$$

If the capacitance decrease or increase at the same rate, the stored data will be retained after 10 years at room temperature. This time dependence is similar to the switching charge loss of imprinted capacitor.[3]

In the FFRAM cell, the stored data disappeared in several hours. The STN capacitors were very small (about $3 \sim 4\mu m^2$), so the leakage current flows at the edge of the capacitor and the stored charge vanishes. This problem will be overcame by optimizing the etching condition of the STN and electrodes.

4. Conclusion

The MFMIS capacitors and FFRAM cells were fabricated using STN thin films.

STN capacitors showed well saturated P–V hysteresis and no inter-diffusion were observed after crystallization annealing from. C–V and I_D–V_G hysteresis curves witch were caused by ferroelectric polarization reversal were observed.

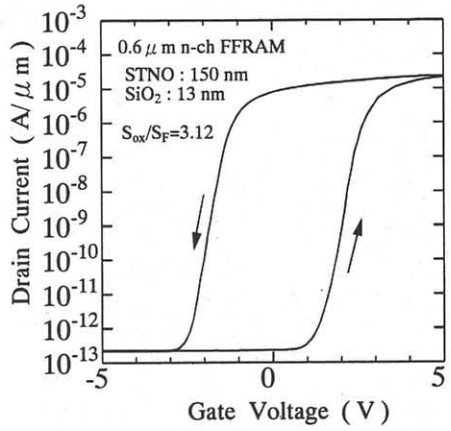

Figure 5: I_D–V_G characteristics of FFRAM cell using STN thin films.

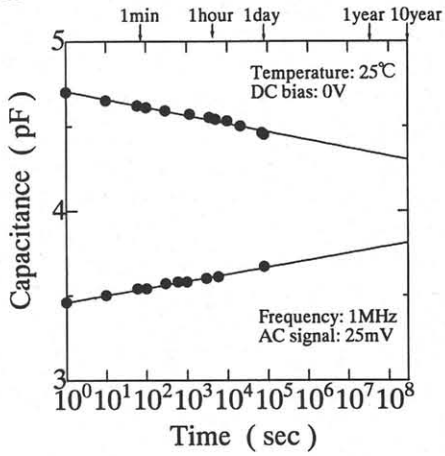

Figure 6: Retention characteristics of the MFMIS capacitor using STN thin films.

In the MFMIS capacitor, the data retention characteristics were shown. The capacitance changed along logarithm of the retention time.

Acknowledgments

The authors would like to thank Mr. Katsumi Ogi and the other staff of Mitsubishi Materials Corporation for supply of ferroelectric source materials.

References

1) Y. Fujimori, N. Izumi, T. Nakamura, A. Kamisawa and Y. Shigematsu: Jpn. J. Apply. Phys. **36** (1997) 5935.

2) T. Nakamura, Y. Nakao, A. Kamisawa and H. Takasu: *Integrated Ferroelectrics* **9** (1955) 179.

3) T. D. Hadnagy: *Integrated Ferroelectrics* **18** (1997) 1.