Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 226-227

Realization of Adaptive Learning Function for Neuron Oscillation Circuit Using Metal-Ferroelectric-Semiconductor(MFS) FET

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1. Introduction

Recently, neural networks with adaptive learning function as human brain have attracted much attention. For the realization of practical neural networks, a simple exclusive hardware system with reasonable learning time is required. We have proposed a novel neuro-device composed of a ferroelectric gate FET (MFSFET) and a unijunction transistor (UJT) oscillation circuit,[1] and reported the basic characteristics of neuron oscillation circuits using conventional MOSFET.[2] It is very difficult to preserve ferroelectricity on Si due to existence of interfacial traps and/or interdiffusion of the constituent elements so that the fabrication process of good MFSFETs is not yet established. This problem is more serious in fabrication of integrated circuits including MFSFETs. In this paper, we report the fabrication of an MFSFET neuron circuit and present the fundamental adaptive-learning operations in neuron oscillation circuits using MFSFET.

2. Basic operation and fabrication process of adaptive learning neuron circuits using MFSFETs.

A basic circuit of pulse frequency modulation (PFM) type neuron circuit is shown in Fig. 1. In this circuit, complementary unijunction transistor (CUJT) is used as a switching component to discharge the capacitor C, in other words, it accomplishes the threshold processing in the summation operation of neural network. The term of 'adaptive learning' means the function that the electrical properties of device are changed partially or totally by applying a certain number of usual signals to the device. This function can be realized by controlling the polarization value of the ferroelectric gate in the MFSFET. In these applications, we can change gradually the S-D (source-drain) resistance of the MFSFET by applying signal pulses, the duration time of which is sufficiently shorter than the switching time for polarization reversal. Therefore, the MFSFET is a key device for storing synaptic weights in the proposed neural network.

This circuit is necessary to be fabricated in an SOI (silicon-on-insulator) structure in this study, since CUJT is a positive feedback device. As a result, each device can be electrically isolated so that the circuit is not latched-up. Every device was fabricated by using 5 μm design rule. $SrBi_2Ta_2O_9$ (SBT) was selected as the ferroelectric gate material for the possibility of direct deposition on Si without critical degradation and deposited by liquid source misted chemical deposition (LSMCD) method for the better step coverage on Si with surface steps. Channel length and width of MFSFET were designed to be 5 μm and 50 μm, respectively. Although metal was patterned using conventional Al, the gate electrode material was formed by Pt lift-off process. The full fabrication processes were devised so that the process damage to ferroelectric gate can be minimized. In other words, the implantation and activation annealing processes were finished before the deposition of ferroelectric gate, and after depositing it, only dry etching process was used. Impurity concentration of CUJT active region was controlled so that oscillation pulse frequency is modified in high frequency region. Furthermore, it is important that the S-D resistance of MFSFET meets the negative resistance range of CUJT. Capacitors were designed to be 3 pF, 10 pF and 30 pF, and R_L was set to 200 Ω~300 Ω. A photograph of the fabricated neuron circuit is shown in Fig. 2.

3. Adaptive learning functions of neuron oscillation circuit using MFSFET.

Figure 3 shows the drain current (I_D)-gate voltage (V_G) characteristic of a fabricated MFSFET. A hysteresis loop was obtained with a counter-clockwise trace, which is believed to be due to the ferroelectricity of SBT gate oxide. The memory window, i.e. threshold voltage shift was 0.45 V for a V_G sweep from 0 V to 6 V. Next, to examine the gradual learning effect when the pulse input signal was applied to gate terminal of this MFSFET, drain current (I_D)-drain voltage (V_D) characteristics were measured by varying the number of pulses. The width and amplitude of applied pulses are 20 ns and 6 V, respectively. A negative pulse with -8 V amplitude was applied between each measurement for initialization of polarization. The I_D increases as the number of applied pulses when the V_G is adjusted at 1.8 V (read voltage), as shown in Fig. 4. It can be said from this result that the polarization of the ferroelectric SBT gate is gradually reversed by pulse signal with sufficiently short duration time, and that the value of V_D for MFSFET (S-D channel conductance) can be controlled by the number of input signals. Therefore, we can expect that the output pulse frequency of neuron oscillation circuit using this MFSFET is simply modulated with non-volatility by applying adequate number of input signals.

Although all fabricated devices were confirmed to operate normally, the integrated circuit failed to accomplish the normal oscillation operation due to one problem. We found that the voltage drop speed during discharging action

for capacitors fabricated in the structure of Al/SBT/SiO_2/Si was not sufficient for CUJT turn-off, which is considered to be attributed to the polarization effect of ferroelectric SBT films. For this reason, we made the measurements using the fabricated MFSFET and CUJT oscillation circuit integrated on another substrate with Al/SiO_2/Si capacitors. From the measurement using DC input signal, the oscillation circuit was found to operate from 3 V to 6 V of V_G applied to MFSFET. Figure 5 shows the modulated wave forms of output pulse after the write input signals of 6 V with 20 ns-width were applied once or 60 times, respectively. The read voltage was adjusted to 2.6 V, at which the neuron circuit cannot show the oscillation operation without applying any write pulse of 6 V. The output pulse frequency change was obtained as a function of the number of input signals applied to MFSFET, as shown in Fig. 6. As the progress of polarization reversal for the ferroelectric gate, the output pulse frequency for the oscillation circuit is increasing. This curve corresponds to the learning characteristic for adaptive-learning neuron oscillation circuits.

4. Conclusion

We have presented the adaptive-learning function for the fabricated neuron circuit using MFSFET and CUJT oscillation circuit. The gradual change of drain current value for MFSFET could be obtained by applying short input pulse signals to ferroelectric gate. Using this gradual increase in S-D conductance of MFSFET, output pulse frequency for neuron circuit could be successfully modulated at the same read voltage. At present, we are improving the fabrication process to solve the above stated problem for integrated circuits.

Acknowledgements

This work was partly supported by Grant-in-Aid for Scientific Research in Priority Areas (No. 07248105) and COE Research (No. 07CE2003, "Ultra-parallel optoelectronics") and a Grant-in-Aid for Scientific Research (B) (No. 9450123) from the Ministry of Education, Science, Sports and Culture.

Reference

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2) S. M. Yoon, E. Tokumitsu, and H. Ishiwara : Jpn. J. Appl. Phys. **37** (1998) 1110

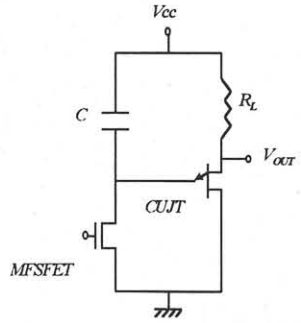

Fig.1 A basic neuron circuit using MFSFET.

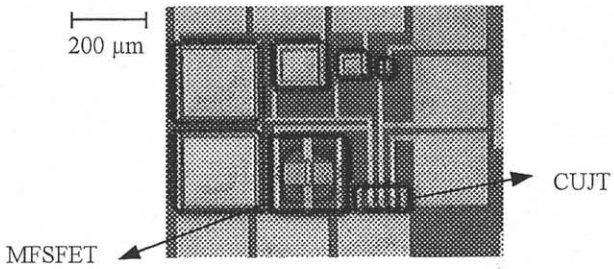

Fig. 2 A photograph of the fabricated neuron circuit.

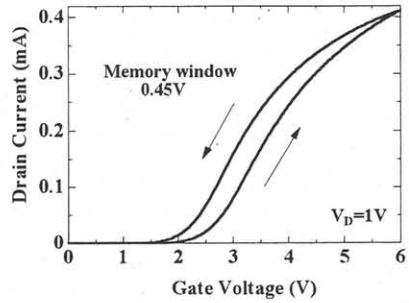

Fig. 3 I_D-V_G characteristic of the fabricated MFSFET.

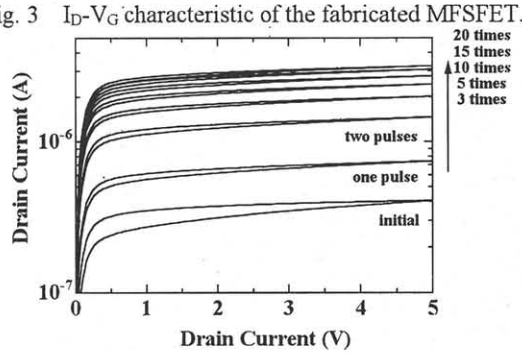

Fig. 4. I_D-V_D characteristics for the MFSFET when the read gate voltage is 1.8 V after applying a certain number of pulses to the gate terminal.

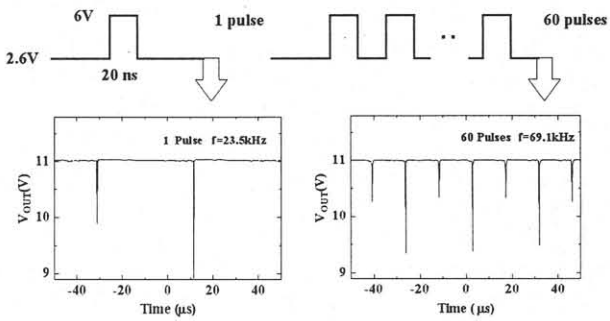

Fig. 5. Wave forms of output pulse for oscillation circuit after the write input signals were applied once or 60 times.

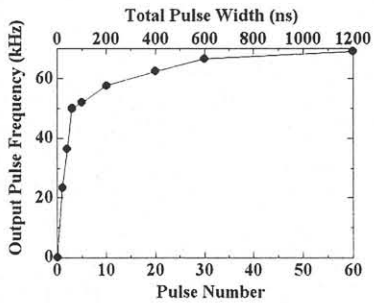

Fig. 6. Change of output pulse frequency as a function of the number of input signals.