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Digital Circuits Based on Single Flux Quanta

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1. Introduction

Recently, many Josephson LSI circuits have been fabricated using integration technology based on the superconducting materials of Nb and NbN. The operation modes of some of these LSI circuits are related to the quantum-mechanical quantization of magnetic flux ($\Phi_0 = h/2e$). For the RSFQ (rapid single-flux-quantum) logic family [1], many kinds of logic circuits, each composed of a few thousand Josephson junctions, have been fabricated and measured experimentally at clock frequencies over 10GHz [2, 3]. Simple circuits of this family have been estimated, from the measurement of the dc voltage across the junction, to operate at frequencies up to 370GHz [4]. For the Phase-Mode Logic family [5, 6], an ICF (INHIBIT controlled by fluxon) gate, a combination of the T- and S- branches, is proposed as the basic element. The ICF gate can be easily configured to perform as a full adder. A complete computer system has been also proposed [6] in the Phase-Mode system. In this paper we present the experimental results on the phase-mode logic circuits and numerical estimations using high critical current density (J_c) of Josephson junctions for a high-speed operation. Moreover, we also present circuit area reduction methods using effective inductance of Josephson junctions, overdumped junctions, and junction-type resistors.

2. Phase-Mode Circuit

Some digital circuits have been fabricated using the first type of ICF gates which requires resistive ground plane contacts. Figure 1 (a) shows a microphotograph of a single-bit adder circuit [7]. The circuit was fabricated using the equipments of the Electrotechnical Laboratory (ETL).

The design values of the J_c and the sheet resistance are 1.0kA/cm^2 and 1.0Ω/square, respectively. The minimum size of Josephson junction is 5×5μm^2. Figure 1 (b) shows the experimental low-speed test result. The fluxon generator (FG) and the fluxon detector (FD) developed by us are used for generating and detecting a fluxon [8]. In Fig. 1 (b), a fluxon is generated at the rising edge of the input current for the FG. The output of the FD arises when it detects a fluxon. The FD is reset by another signal which is not shown in Fig. 1 (b). Details of the experiment are described in Ref.[7].

Though the ICF gate of the first type has wide margins, ground coupling resistors (and their contact holes) should preferably be removed from an integration point of view. It is possible to use another type of circuit. However, the spread of the bias margins of the second type is larger than that of the first type, because the operation sequence is more complex than that of the first type. The first type has some advantages in variations of circuit parameters.

Let us discuss the high-speed operation of the phase-mode logic circuits with high-J_c Josephson junctions. Recently, high-J_c Nb/AlO$_x$/Nb junctions of several hundreds of kA/cm^2 have been reported. Utilization of such high-J_c junctions decreases the switching delay of the

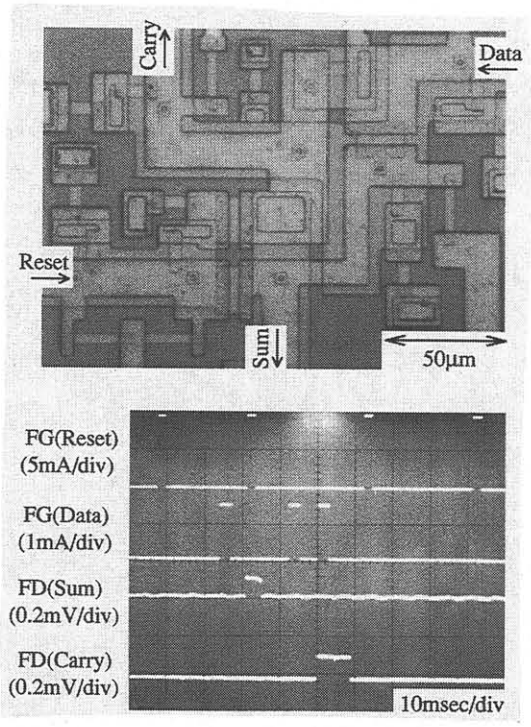

Figure 1: Single-bit adder circuit. (a) Microphotograph. (b) Logic operation. The top, the second, the third, and the bottom lines represent the input current for the FG(Reset), the input current for the FG(Data), the output voltage of the FD(Sum), and the output voltage of the FD(Carry), respectively.

phase-mode circuits.

Measurement of dc average voltage across junctions is a simple method for evaluating operation frequency, because the dc voltage is converted to the frequency by using the Josephson voltage-frequency relation. We have experimentally investigated the operation frequency of the adder circuit shown in Fig. 1 using the dc voltage measurement method [7]. The result indicates that the carry operation follows up to 99GHz input pulses. Figure 2 shows the maximum input dc voltages for the carry operation as a function of the bias current. The experimental results and simulated results for J_c of 1.0kA/cm^2 and 100kA/cm^2 are also plotted. The simulations for ICF gates with 100kA/cm^2 Nb/AlO$_x$/Nb parameters show that the gate delays are about 0.5ps and about 2ps for the first and the second types of ICF gate, respectively. There is a discrepancy between the experimental results and the simulation for J_c=1.0kA/cm^2 in Fig. 2. We speculate that the discrepancy is mainly due to insufficient damping for the junctions.

The ratio of the critical current to the minimum current returning to the zero voltage state is about 1/0.75 for J_c=500kA/cm^2 (12μF/cm^2). The numerical simulation of the second type of ICF gate with 500kA/cm^2 Nb/AlO$_x$/Nb junctions shows that we can remove shunt resistors in a phase-mode circuit if extremely high-J_c junctions are available.

The phase-mode circuit consists of Josephson junctions, resistors, and inductors. In actual integrated circuits, inductors occupy a large part of the chip area. Application of the effective inductance of a Josephson junction is one of the better contenders for reducing the inductance area. Phase-mode circuits can take advantage of the effective inductance, because the circuit connection with magnetic coupling is not required.

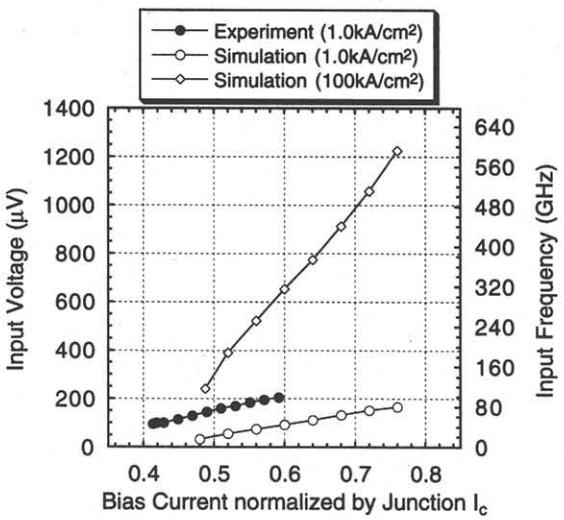

Figure 2: Maximum input frequency for the carry operation as a function of the circuit bias current. The simulated results are for J_c of 1.0kA/cm^2 (C_s = 5.0μF/cm^2) and J_c of 100kA/cm^2 (C_s = 8.8μF/cm^2). All resistors for J_c=100kA/cm^2 are 7.5 times larger than those for J_c=1kA/cm^2.

In the phase-mode circuits, nonhysteretic junctions are necessary for stabilizing the fluxoid motion. It is possible for a Nb/AlO$_x$-Al/Nb junction to possess such characteristics following addition of a metallic resistor. However, S-N-S-like junction without shunt resistor (intrinsically overdumped junction) is useful for high-density integration. We have fabricated Nb/AlN$_x$/Nb junctions to realize the S-N-S-like junctions. The J_c and the characteristic voltage are 2.3kA/cm^2 and 0.20mV, respectively. We can also propose the realization of compact circuit integration by replacing the plane metallic resistor with the normal resistance of the junction.

The area of layout is estimated to be half if we use the Nb/AlN$_x$/Nb junctions of J_c=1kA/cm^2 with 10μm line width. On the other hand, it is almost the same as that of the Nb/AlN$_x$/Nb junction case whether we use the effective inductance or whether we do not. However, the reduction ratio of the layout increases with increasing J_c, because the fringe factor of the strip line inductor increases rapidly with decreasing line width. Therefore, the inductor junctions give large effects in the submicrometer integration scale which results in 0.52% circuit area for J_c=100kA/cm^2 which gives 1μm line width of inductors.

The new design and preliminary experiments for high-performance phase-mode logic circuits have been presented. The results indicates that the carry operation follows up to 99GHz input pulses. We have also numerically investigated the applicability of high-J_c Josephson junctions to phase-mode circuits. The carry operation can perform up to 592GHz for J_c=100kA/cm^2. Furthermore, we have discussed a new technology for reducing the integration area of phase-mode circuits.

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