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Stress-Induced Leakage Current and Lateral Non-Uniform Charge Generation In Thermal Oxides Subjected to Negative-Gate-Voltage Impulse Stressing

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1. Introduction

High-field stressing during the write/erase cycles in non-volatile semiconductor memories (NVSMs), such as EEPROMs and Flash devices, can lead to an increase in the stress-induced leakage current (SILC) [1,2]. The SILC increases with decreasing oxide thickness [2], and thus imposes a potential scaling limitation for tunnel oxide applications in NVSMs. The SILC has been shown to result from trap-assisted tunneling [2-4]. DiMaria has previously studied the effect of positive-gate-voltage Fowler-Nordheim (FN) tunneling stress on 4 to 10 nm thick oxides and concluded that lateral non-uniform (LNU) hole-trapping effects were not observed [5]. In our previous investigation on trap generation in 8 and 13 nm thick oxides under positive-gate-voltage high-field impulse stressing to simulate electrostatic discharge (ESD) stress conditions, we did not observe any LNU charge generation in the MOS capacitor structures [6], which is consistent with [5]. Recently, we observed LNU charge generation in silicon dioxide under negative-gate-voltage impulse stressing. The LNU charge is related to SILC.

2. Experimental Details

The thermal-oxide capacitor test structures, having an oxide thickness (t_{OX}) of 14.7 nm and gate areas of 50000, 200000 and 815000 μm^2, were fabricated in an n-well on a (100) p-type silicon substrate. The gates of the MOS capacitors were stressed with negative voltage pulses of 24 to 27 V magnitude and 200 ns duration using a transmission line pulsing (TLP) technique [7]. The current density during the 200 ns high-field pulse is about 40 to 50 A/cm^2.

3. Results and Discussion

High-frequency (f = 100 kHz) capacitance-voltage (HF C-V) measurements showed distortion in the depletion region after the negative-gate-voltage high-field stress as seen in Fig. 1(a). Conductance measurements on the negative-gate-voltage impulse-stressed oxides and oxides subjected to constant voltage Fowler-Nordheim (F-N) stressing, to intentionally create interface states, showed that the HF C-V curve distortion is due to LNU charge and not interface states. The HF C-V curves in Fig. 1(a) show that the generated LNU charge is positive in nature as seen from the distortion in the C-V characteristics towards negative gate voltages. The appearance of the LNU charge after negative-gate-voltage impulse stressing in Fig. 1(a) correlates with the SILC in Fig. 1(b). The LNU charge and SILC can be electrically annealed through repeated J_g-V_g meausrements The inset in Fig. 1(b) shows that the increment in the SILC is correlated with the amount of LNU charge annealed. The LNU charge can also be electrically annealed either using a positive-gate-voltage CVS step or a constant current stress (CCS). The CVS annealing results in Fig. 2 show that the amount of LNU charge annealed has a logarithmic dependence with the annealing time. The rate of annealing of the LNU charge, which can be estimated from the slope of the plots in Fig. 2 and shown in the inset, increases rapidly when the annealing gate voltage increases from 2 to 4 V, stays relatively constant for the 4 to 6 V range, and then increases again for gate voltages greater than 6 V. Figure 3 shows that there is a logarithmic relation between the amount of LNU charge annealed and the injected fluence (Q_{inj}) during the CVS annealing. The amount of annealing per injected fluence is also higher for a larger gate voltage. Figure 4 shows constant-current annealing under positive I_g (substrate electron injection) and negative I_g (gate electron injection). After some critical annealing time (t_c), the amount of annealing increases significantly. t_c is smaller for substrate electron injection ($t_c \sim 136$ and 181 s for I_g = +35 and +25 pA respectively) than for gate electron injection ($t_c \sim 304$ and 405 s for I_g = -35 and -25 pA respectively). Under conditions of gate electron injection, the surface of the semiconductor is in a depleted/inverted condition and part of the voltage is dropped across the depletion, which means a smaller voltage drop across the oxide for the same value of annealing current as compared to substrate electron injection. This suggests that significant annealing of the LNU charge only occurs after some minimum voltage or field is built up across the oxide. By monitoring the voltage across the capacitor at the critical time or the onset of significant LNU charge annealing for the case of substrate injection (i.e. accumulation condition), it is estimated that this critical oxide voltage drop is about 3 V, corresponding to an oxide field of about 1.86 MV/cm. The amount of injected fluence before significant annealing of the LNU charge began was found to be about two times larger for gate injection than for substrate injection. This suggests that the LNU charge is located closer to the oxide-silicon interface. For gate injection, more electrons will be lost by scattering and other loss mechanisms in the oxide and less will be available for annealing as the LNU charge is located further away from the electron injection interface. Previous works have linked the SILC to positive charge generation [8] and neutral trap generation [2, 4] through various trap-assisted tunneling processes [2-4, 9]. Our results showed that the SILC is related to the positive LNU charge. We have shown previously [6] that positive-gate-voltage high-field impulse stressing results in the formation of hole traps and neutral electron traps in equal quantities as both types of traps originate simultaneously from the cleavage of the Si-O-Si bond. Hole trapping is also observed during negative-gate-voltage high-field impulse stressing; hence neutral electron traps will be generated at the same time. It is suggested that the positive LNU charge could be some form of stress-generated neutral electron traps which subsequently trap a positive charge. The fact that significant annealing of the LNU charge occurs only after a certain minimum voltage is applied across the device or after a certain critical time under constant-current annealing suggests that the traps (which could be distributed with multiple energy levels in the oxide), responsible for the LNU charge, have some minimum energy level. Only when the minimum voltage applied results in the Fermi level in the cathode to be higher than the trap energy will electron tunneling takes place from the cathode to neutralize the positive LNU charge.

4. Conclusion

The generation of positive LNU charge in silicon dioxide subjected to negative-gate-voltage, high-field impulse stressing was observed and found to be correlated to the SILC. The LNU charge and SILC can be electrically annealed through repeated J_g-V_g measurements or using either a constant-voltage or constant-current stress step. The electrical annealing studies show that the positive LNU charge is located close to the oxide-silicon interface and distributed with a certain minimum energy level.

References

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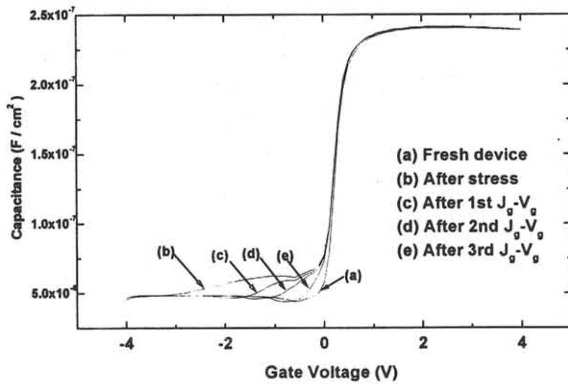
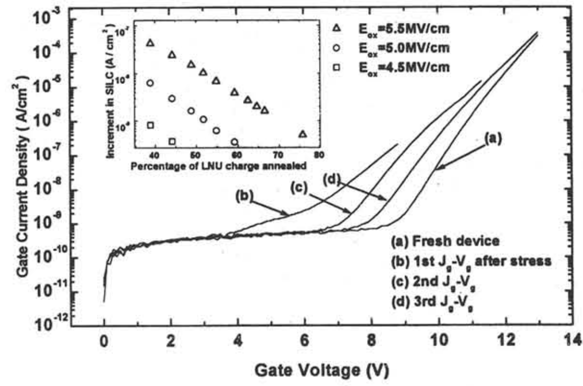


(a)



(b)

Figure 1: Generation and electrical annealing of the lateral non-uniform (LNU) charge and stress-induced leakage current (SILC) in the 14.7 nm thermal-oxide capacitor test structures. (a) High frequency (HF) capacitance-voltage (C-V) measurements (f = 100 kHz) on the fresh device (curve 'a'), after negative-gate-voltage impulse stressing (curve 'b') and after the repeated I_g-V_g measurement (curves 'c', 'd' and 'e'). The negative-gate-voltage impulse stressing is performed by applying 70 pulses of -24 V and 200 ns duration to the gate electrode. (b) J_g-V_g measurement on fresh device (curve 'a'), the negative-gate-voltage stressed device (i.e., first J_g-V_g measurement after impulse stressing, indicated by curve 'b') and subsequent J_g-V_g measurements (indicated by curves 'c' and 'd'). The gate current density was limited to 10^{-7} A/cm² during the J_g-V_g measurements. The inset in (b) shows the increment in the stress-induced leakage current (SILC) (increment obtained by comparing the SILC to that of a fresh device) at oxide electric fields of 4.5, 5.0 and 5.5 MV/cm plotted against the amount of LNU charge annealed.

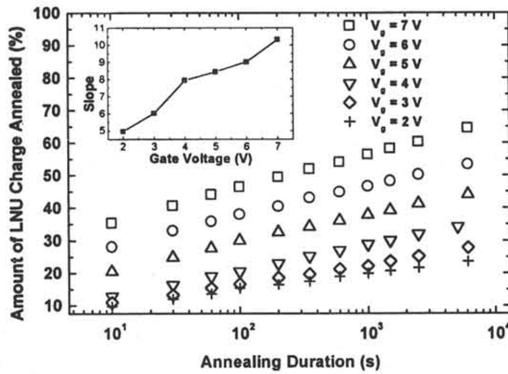


Figure 2: Electrical annealing of the lateral non-uniform (LNU) charge under constant voltage stressing (CVS) conditions for the 14.7 nm thermal-oxide capacitor test structures. The amount of LNU charge annealed after different annealing time durations t, normalised to the LNU charge present at time t = 0 and denoted by $Q_{LNU(normalised)}$, for constant-voltage annealing under positive gate voltages V_g of 2, 3, 4, 5, 6 and 7 V are shown. The respective oxide electric fields (E_{OX}) during the CVS annealing for these gate voltages are estimated to be 1.18, 1.86, 2.54, 3.22, 3.89 and 4.58 MV/cm. The negative-gate-voltage impulse stressing is performed by applying 100 pulses of -24 V and 200 ns duration to the gate electrode. The rate of LNU charge annealing, estimated from the slopes of the plots, is plotted against the annealing gate voltage in the inset.

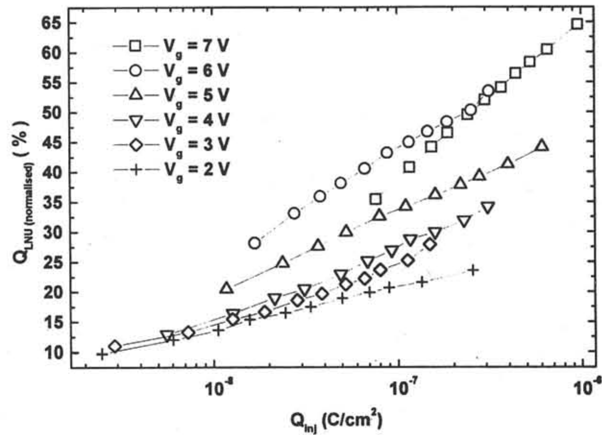


Figure 3: The amount of LNU charge annealed $Q_{LNU(normalised)}$ versus the cumulative injected charge density or fluence Q_{inj} for constant-voltage annealing under positive gate voltages V_g of 2, 3, 4, 5, 6 and 7 V for the 14.7 nm thermal-oxide capacitor test structures. The respective oxide electric fields (E_{OX}) during the CVS annealing for these gate voltages are estimated to be 1.18, 1.86, 2.54, 3.22, 3.89 and 4.58 MV/cm. The negative-gate-voltage impulse stressing is performed by applying 100 pulses of -24 V and 200 ns duration to the gate electrode.

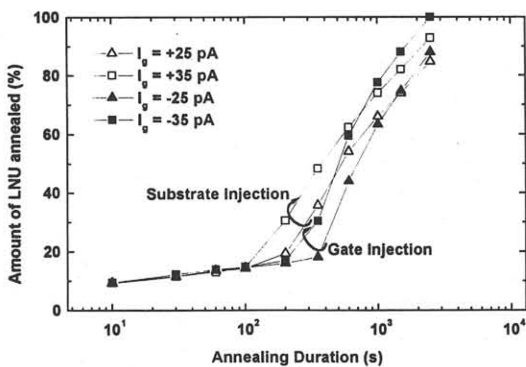


Figure 4: Electrical annealing of the lateral non-uniform (LNU) charge under constant current stressing (CCS) conditions for the 14.7 nm thermal-oxide capacitor test structures. The amount of LNU charge annealed after different annealing time durations t, normalised to the LNU charge present at time t = 0 and denoted by $Q_{LNU(normalised)}$, for constant-current annealing under a gate current I_g of +35 pA and +25 pA (positive sign indicating electron injection from the substrate), and -35 pA and -25 pA (negative sign indicating electron injection from the gate) are shown. The negative-gate-voltage impulse stressing is performed by applying 70 pulses of -24 V and 200 ns duration to the gate electrode.